TECHNICAL MANUAL
FOR
DIGITAL CARRIER ANALYSIS TEST SET
MODEL 273B

PLEASE NOTE
FAILURE TO RETURN THIS MANUAL WILL RESULT IN A MINIMUM BILLING CHARGE OF $50.00.

PLEASE INCLUDE MANUAL AND ACCESSORIES WHEN RETURNING EQUIPMENT

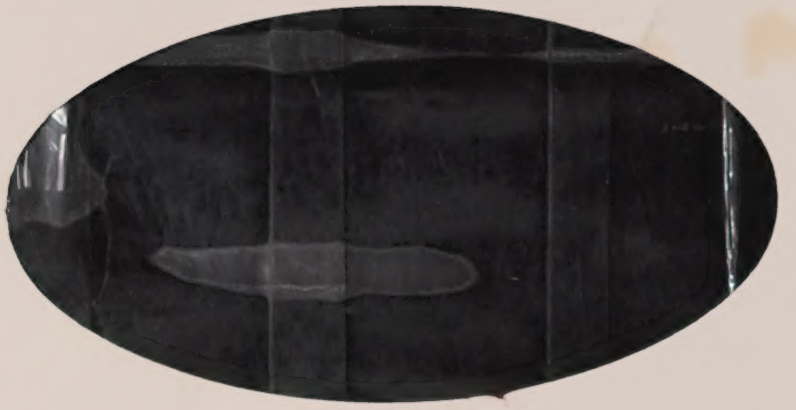
LEASAMETRIC
1166 TRITON DR. • FOSTER CITY, CA 94404

L16 (REV. 04/85)

Bowmar
WHEN QUALITY COUNTS

Communications Test Equipment

Bowmar/ALI Inc.
531 Main Street
Acton, Mass. 01720



TECHNICAL MANUAL
FOR
DIGITAL CARRIER ANALYSIS TEST SET
MODEL 273B

MANUFACTURED BY

BOWMAR/ALI, INC.
531 Main Street
Acton, Massachusetts U.S.A. 01720

Rev. 1
January, 1985

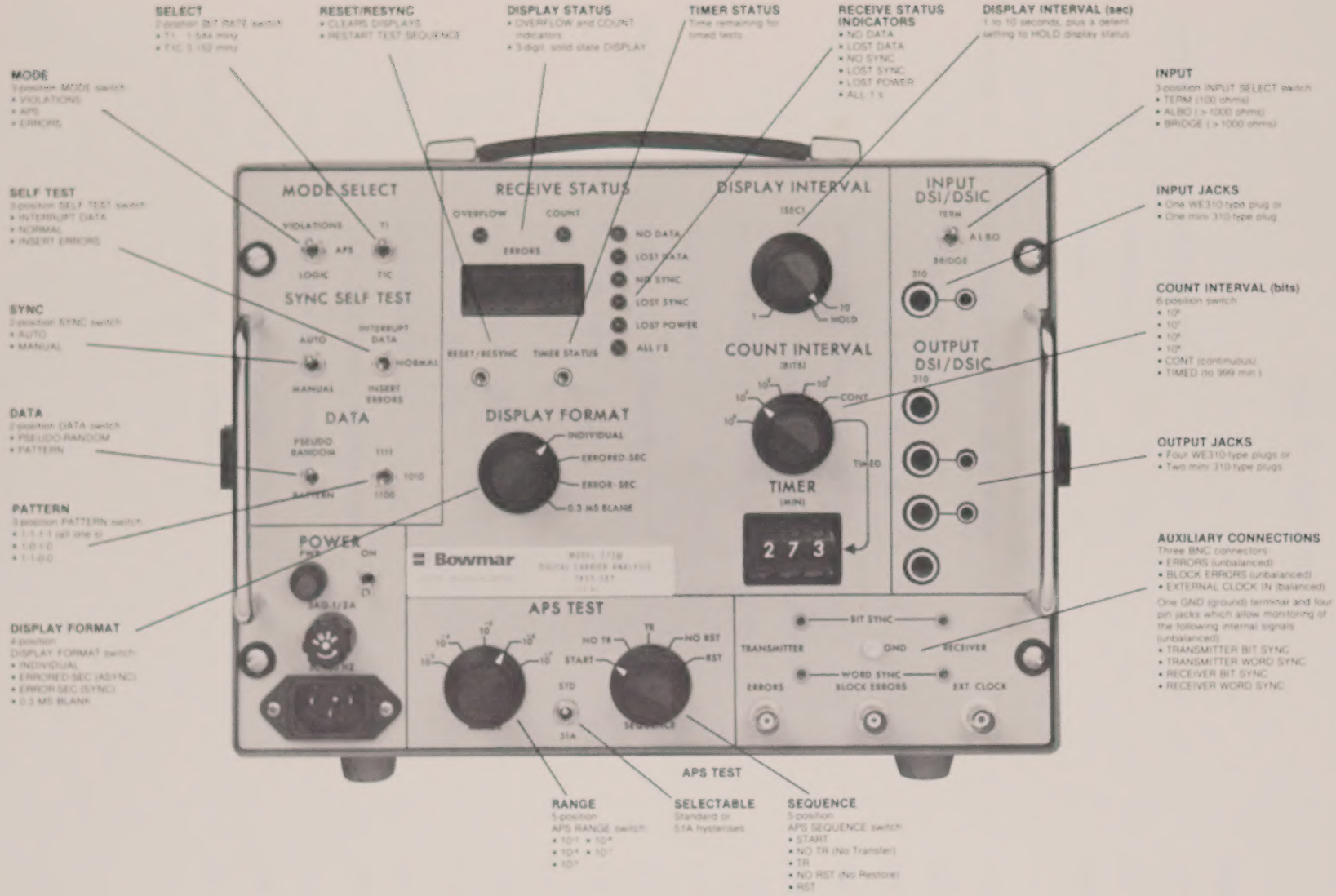
SPECIAL NOTICE

Bowmar/ALI, Incorporated

Proprietary Information

WARNING - Do not copy or distribute.

This technical manual contains proprietary information of Bowmar/ALI, Incorporated and its receipt or possession does not convey any rights to reproduce, disclose its contents, or to manufacture, use or sell in whole or in part anything it may describe. Reproduction, disclosure, or use without the specific written authorization of Bowmar/ALI, Incorporated is strictly forbidden. This restriction does not limit the right to use information contained in this manual if it has been vadidly obtained from another source or has been placed in the public domain without the fault of any person, firm or corporation in possession of this manual.



APS TEST

RANGE
5-position
APS RANGE switch
• 10^{4} • 10^{5}
• 10^{6} • 10^{7}
• 10^{8}

SELECTABLE
Standard or
51A hysterises

SEQUENCE
5-position
APS SEQUENCE switch
• START
• NO TR (No Transfer)
• TR
• NO RST (No Restore)
• RST

MODEL 273B ERROR RATE TEST SET

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_06204

TABLE OF CONTENTS

		PAGE
SECTION 1	INTRODUCTION	1-1
1.1	Description	1-1
1.2	Scope	1-1
SECTION 2	INSTALLATION AND SELF TEST	2-1
2.1	Preparation	2-1
2.2	Check/Self Test Procedure	2-1
SECTION 3	OPERATION AND APPLICATIONS	3-1
3.1	Controls, Indicators, and Connectors	3-1
3.2	Printer/Remote Interface (Option P)	3-7
3.3	Applications	3-12
SECTION 4	THEORY OF OPERATION	4-1
4.1	Transmitter	4-1
4.2	Receiver	4-3
4.3	Transmitter Circuits	4-5
4.4	Receiver Circuits	4-10
SECTION 5	MAINTENANCE	5-1
5.1	Test Equipment Requirements	5-1
5.2	Calibration Procedure	5-2
5.3	Performance Checks	5-6
SECTION 6	DIAGRAMS And SCHEMATICS	6-1

1.0 INTRODUCTION

1.1 Description

The Bowmar/ALI Model 273B Digital Carrier Analysis Test Set is a portable instrument capable of performing a reliable check of T1 (DS-1) 1.544 Mb/s and T1C (DS-1C) 3.152 Mb/s PCM communications systems. Special features include a 0 - 999 minute timer, ALBO (Automatic Line Buildout) permitting measurements at distances ranging from 500 to 4000 feet from the line repeater, standard bridge/terminate inputs for measurements at or within 750 feet of the DSX patch bay or data service unit and APS (Automatic Protection Switch) testing for both standard and 51A switch hystersis.

The 273B transmitter provides four T1 compatible AMI outputs with four data patterns: The 1,048,575 bit quasi-random sequence identical to that provided by AT&T Technologies J98710R T1 quasi-random signal source (QRSS) with a 14 zero constraint, All Ones, Alternating 1100 and Alternating 1010 (blue pattern). At the T1C rate the QRSS sequence is modified to permit consecutive zero strings of up to nineteen "0's". A strap option is provided which will restrict consecutive zeros to fourteen, if desired. The QRSS provides a realistic degree of stress at both the T1 and T1C data rates for the facility under test.

The receiver portion of the instrument operates independent of the transmitter. It performs either bipolar-violation-detection or bit-error-detection on any signal while working in conjunction with its own transmitter or equivalent source. By the use of logic (QRSS) error measurements, the 273B can be used to test any system or system component which remove bipolar violations and/or causes logical errors without causing bipolar violations.

Fully solid state, this instrument includes features such as a self-test, a three digit display with overflow indicator, automatic and manual resynchronization of the logic receiver, error insertion in the transmitter for circuit identification, receiver status indicators, comprehensive count intervals including both block and time selections, and input line selections for bridge, terminate or ALBO operation.

1.2 Scope

This manual contains descriptive details of the Error Rate Test Set plus related applications notes, maintenance information, diagrams, and parts information. The descriptive details are reduced to categories of physical and functional specifications, operating procedures, and operating principles, The manual's purpose is to provide sufficient familiarization to enable effective use and proper maintenance of the Test Set.

SPECIFICATION SUMMARY

OUTPUT PATTERNS:	T1	(a)	A 1,048,575 bit quasi-random pattern limited to 14 consecutive zeros: compatible with Western Electric J98710R Quasi-Random Signal Source.
		(b)	All Ones 1-0-1-0 1-1-0-0
	T1C	(a)	A 1,048,575 bit quasi-random pattern provides for 19 consecutive zero components. A strap option is provided to limit consecutive zeros to 14
		(b)	All Ones 1-0-1-0 1-1-0-0
INPUT:			Balanced; one jack which accepts a WE310-Type plug (T & R) and one jack which accepts a mini 310 (T & R)
INPUT IMPEDANCE:			Terminate 100 ohms Bridge > 1000 ohms ALBO > 1000 ohms
OUTPUTS:			Four balanced outputs distributed by four WE310-Type and two mini 310 jacks (T & R)
Output Impedance:			100 ohms ± 5%
Auxiliary Connectors:			Three BNC: ERRORS (Unbalanced) - TTL (Out) BLOCK ERRORS (Unbalanced) - TTL (Out) EXTERNAL CLOCK IN (Balanced) - Bipolar One GND (Ground) terminal and four pin jacks which allow monitoring of the following internal signals (Unbalanced): TRANSMITTER BIT SYNC TRANSMITTER WORD SYNC RECEIVER BIT SYNC RECEIVER WORD SYNC

CONTROLS:

MODE SELECT Switch	3-position:	VIOLATIONS APS ERRORS
BIT RATE Switch	2-position:	T1 - 1.544 mHz T1C - 3.152 mHz
SYNC	2-position:	AUTO MANUAL
SELF TEST Switch	3-position:	INTERRUPT DATA (momentary - Interrupts Internal Loopback) NORMAL INSERT ERRORS (momentary) (See Para. 2.2.5 thru 2.2.8)
APS TEST Switches:	A. RANGE: 5-position:	10^{-3} 10^{-4} 10^{-5} 10^{-6} 10^{-7}
	B. SEQUENCE: 5-position:	START NO TR (No Transfer) TR NO RST (No Restore) RST
DATA Switches:	A. 2-position:	Pseudo-random Pattern
	B. 3-position:	ALL ONES 1-0-1-0 1-1-0-0
POWER Switch	2-position:	ON OFF
RESET/RESYNC Switch	Momentary Toggle	
TIMER STATUS Switch	Momentary Toggle	
DISPLAY FORMAT Selection Switch:	4-position:	INDIVIDUAL ERRORED SECONDS-(ASYNC) ERROR SECONDS - (SYNC) 0.3 MS BLANK

DISPLAY INTERVAL (SEC) Control:	1 to 10 seconds, plus a detent setting for HOLD
COUNT INTERVAL (BITS):	6-position: 10^6 10^7 10^8 10^9 CONT (Continuous) TIMED
TIMER (minutes) Switches:	RANGE: 1 - 999 minutes
INPUT TERMINATION Switch:	3-position: TERM (Terminated 100 ohms) ALBO (> 1000 ohms) BRIDGE (> 1000 ohms)

INDICATORS:

RECEIVE STATUS Indicators:	6 separate LED indicators: NO DATA LOST DATA NO SYNC LOST SYNC LOST POWER ALL ONES
DISPLAY STATUS Indicators:	2 separate LED indicators: OVERFLOW COUNT
DISPLAY:	3-digit; LED
FUSE and SPARES:	AC POWER: 1 each 3AG, 1/2A, Slow Blow DC POWER: 1 each 3AG, 3/4A, Slow Blow Spare fuses located in cover.
POWER SOURCE:	117 VAC ± 10%, 47 to 63 Hz, Single Phase or 48 VDC ± 4 VDC positive ground to sleeve, negative 48 to Tip. WE410 Type plug.
RECEIVER INPUT THESHOLD:	Bridge and terminate: 0.2 to 6.0V peak; automatic threshold control for operation at DSX MONITOR jack, cross-connect bay or up to 750 feet from source. ALBO: Correction for 500 to 4000 ft. PIC, PULP or ABAM cable driven by a ± 3V peak bipolar source.
SYNC ACQUISITION TIME:	Less than 200 clock pulses. (Test Set will not resync on isolated error bursts of less than 6 consecutive errors).

PRINTER INTERFACE OPTION P (273B-1P)	Fifty pin mini blue ribbon connector format; Three parallel BCD digits with print and test set control commands.
TRANSMITTER OUTPUT T1 BIPOLAR PULSE CHARACTERISTICS:	
Height of Output Pulse:	3V ± 0.3V
Unbalance in Height of Negative and Positive Pulse:	0.15V
Overshoot at Trailing Edge of Pulse:	10 to 30% of pulse height with decay of 10% or less of base line-to-peak value within 400 nsec.
Width of Output Pulse (Half Amplitude):	324 ± 30 nsec
Unblance in Width of Negative and Positive Pulse:	± 15 nsec
Maximum Rise or Fall Time:	80 nsec
TRANSMITTER OUTPUT T1C BIPOLAR PULSE CHARACTERISTICS	
Height of Output Pulse:	3V ± 0.3V
Unbalanced in Height of Negative and Positive Pulse:	0.15V
Overshoot:	Less than 10% of Pulse Height
Width of Output Pulse (Half Amplitude)	160 nsec ± 15 nsec
Unbalance in Width of Negative and Positive Pulse:	± 15 nsec
Maximum Rise or Fall Time:	40 nsec
OPERATING ENVIRONMENT:	0 to 50°C (32 to 120°F) to 95% relative humidity

2.0 INSTALLATION AND SELF TEST

2.1 Preparation

2.1.1 Remove the Digital Carrier Analysis Test Set from its shipping container.

2.1.2 Remove the front cover.

2.1.3 Check for the presence of 3AG, 1/2A, (Front Panel) and 3AG, 3/4A (Rear Panel) slow blow fuses.

2.1.4 Remove the power cord from the front cover and connect the Test Set to a 115V ac, 50-60 Hz, single-phase power source.

2.1.5 Set the POWER switch to ON and note whether or not the indicator illuminates.

2.2 Check/Self Test Procedure

2.2.1 Set switches to the following initial positions:

MODE	-to VIOLATIONS
DATA	-to PSEUDO-RANDOM
DISPLAY FORMAT	-to INDIVIDUAL
(BIT RATE) SELECT	-to T1
SYNC	-to MANUAL
DISPLAY INTERVAL (SEC)	-to "1" (full counterclockwise)
COUNT INTERVAL (BITS)	-to "10^6"
RESET/RESYNC	-to Momentarily Actuate and Release

2.2.2 Observe indicators for the following initial responses:

NO DATA	-OFF
LOST DATA	-OFF
NO SYNC	-ON
LAST SYNC	-ON
LOST POWER	-OFF
ALL 1's	-OFF
OVERFLOW	-OFF
COUNT	-Alternately on for approximately 2/3 second, off for approximately 1 second
DISPLAY	-"0" (Constant)

2.2.3 Turn the DISPLAY INTERVAL (SEC) control clockwise to the '10' position. The COUNT indicator should alternately be ON for approximately 2/3 second and OFF for approximately 10 seconds.

2.2.4 Place the DISPLAY INTERVAL (SEC) control in its HOLD (detent) position and momentarily operate the RESET/RESYNC switch. The COUNT indicator should come ON for approximately 2/3 second and then remain OFF. indefinitely. Check the off condition for at least twenty seconds.

2.2.5 Place the DISPLAY INTERVAL (SEC) control at some point between '1' and '5'. Hold the SELF TEST switch at its INSERT ERRORS position. The count on the Display should change by increments of two from a starting count of '0' to a final count of '8' while the COUNT indicator is ON. At the count of '8', the Display should hold for the period set by the DISPLAY INTERVAL (SEC) control, then it should clear to '0' and begin a new cycle. The first count interval may not yield a total of eight errors, but each succeeding interval should register a count of '8' on the Display.

2.2.6 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^6 to 10^7. The count on the Display should perform as it did in Step 2.2.5 above, however, a full count interval should now register '80'.

2.2.7 *Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^7 to 10^8. The count on the Display should perform as it did in Steps 2.2.5 and 2.2.6 above, however, a full count interval should now register '800'.

2.2.8 *Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^8 to 10^9. The count will stop after approximately 11 minutes and 21 seconds. The Display should cycle through a complete count of 0 to 1000, a total of eight times. Since the Display contains only three digits, a count of 1000 will register as '0' with an OVERFLOW indication. The OVERFLOW indicator should come ON at the first count of 1000. It will remain on after this point through the remaining seven cycles of 0 to 1000.

2.2.9 Holding the SELF TEST switch at its INSERT ERRORS position, change the COUNT INTERVAL (BITS) switch from 10^9 to CONT position and momentarily operate the RESET/RESYNC switch. The count on the Display should accumulate as in the preceding steps, and the OVERFLOW indicator should come ON as the Display goes from '998' to '0' and stay ON. Check that count continues for at least 12 minutes after OVERFLOW indicator comes ON.

2.2.10 While holding the SELF TEST switch at its INSERT ERRORS position, momentarily operate the RESET/RESYNC switch. As it is operated the Display should clear to '0', and the OVERFLOW and COUNT indicators should go OFF; the COUNT indicator should come ON again within 2/3 second of Switch release.

2.2.11 Change the COUNT INTERVAL switch from CONT to TIMED. Hold both the RESET/RESYNC and TIMER STATUS switches in their momentary position. Rotate each of the TIMER thumbwheel switches through their ten positions noting a correlation between the DISPLAY and SWITCH position.

*Optional unless trouble suspected

2.2.12 Set the TIMER switch to 001 and momentarily operate the RESET/RESYNC switch. The COUNT INDICATOR should stay on for a period of one minute. The Display should read '0' when the TIMER STATUS switch is operated after the COUNT indicator's transition to the OFF state.

2.2.13 Return the COUNT INTERVAL (BITS) switch to its 10^6 position.

2.2.14 Set the MODE switch at LOGIC and momentarily operate the RESET/RESYNC switch. The Display indication should be '0' and all RECEIVE STATUS indicators should be OFF.

2.2.15 Push and hold the SELF TEST switch to INTERRUPT DATA. The NO DATA and NO SYNC indicators should come ON. The LOST DATA and LOST SYNC indicators should remain OFF.

2.2.16 Release the SELF TEST switch. The NO DATA indicator should go OFF, the LOST DATA and NO SYNC indicators should be ON, and the LOST SYNC indicator should be OFF. The Display should show '000' with an OVERFLOW indication during the COUNT INVERVAL, and any number with OVERFLOW at the end of the COUNT INTERVAL.

2.2.17 Place the SYNC switch to the AUTO position. The NO SYNC indicator should go OFF and the LOST SYNC indicator should come ON. The LOST DATA indicator should remain ON. The Display should register '0' without OVERFLOW.

2.2.18 Momentarily operate the RESET/RESYNC switch. The LOST SYNC and LOST DATA indicator should go OFF.

2.2.19 Push and hold the SELF TEST switch at INSERT ERRORS. The Display should change by increments of two to a final count of '8'.

2.2.20 Change the COUNT INTERVAL (BITS) switch to the TIMED position. Set the TIMER switches to one minute ('1'). Set the DISPLAY FORMAT switch to the ERRORED-SEC position.

2.2.21 Hold the SELF TEST switch in the INSERT ERRORS position and momentarily operate the RESET/RESYNC switch. The COUNT indicator should come ON for a period of one minute. After the count interval is complete, the Display should register between '59' and '61'.

2.2.22 Change the COUNT INTERVAL (BITS) switch to 10^7 and the DISPLAY FORMAT switch to ERROR-SEC.

2.2.23 Hold the SELF TEST switch in the INSERT ERRORS position and momentarily operate the RESET/RESYNC switch. The Display should count by increments of one to a final count of '7'.

2.2.24 Change the DISPLAY FORMAT switch to 0.3 ms BLANK.

2.2.25 Hold the SELF TEST switch in the INSERT ERRORS position. The Display should count by increments of one to the final count of '40'.

2.2.26 Change the BIT RATE switch to T1C and DISPLAY FORMAT switch to INTEGRAL.

2.2.27 Operate the RESET/RESYNC switch. ALL RECEIVER STATUS indicators should be OFF and the Display should register '0' without OVERFLOW.

2.2.28 Hold the SELF TEST switch in the INSERT ERRORS position and momentarily operate the RESET/RESYNC switch. The Display should count in increments of two for a final count of '80'.

2.2.29 Return the (BIT RATE) SELECT switch to the T1 position.

2.2.30 Determination of the operational readiness of the Test Set when operating in the APS TEST mode requires the use of an external bipolar signal source and bipolar violations detector. Another 273 or the Bowmar Model 271A (KS-20775 L1), 271B, or 271C (KS-20775 L2) Error Rate Test Set may be used to fulfill this requirement. A Bowmar Model 271C will be used for the purpose of outlining a general test procedure.

Using patch cords with WE 310-type plugs at each end, connect a DS1 OUTPUT of the 271C to the DS1 INPUT of the 273 under test; connect any DS1 OUTPUT of the 273 under test to the DS1 INPUT of the 271C.

Set the MODE switch on the 271C to the VIOLATIONS position, COUNT INTERVAL BITS switch to 10^6 and BLOCK ERROR switch to OUT. Momentarily operate the RESET/RESYNC switch. The NO SYNC and LOST SYNC indicators should be ON.

Set the MODE switch on the 273 to APS, and momentarily operate the RESET/RESYNC switch. The Display should be blanked with the NO SYNC and LOST SYNC indicators ON.

The following Table lists a set of APS switch combinations which will completely test this function. Each APS switch combination is followed by a COUNT INTERVAL switch setting and display response pertaining to the testing instrument (271C). Complete each step of the Table, observing that each result complies with the Table's requirement.

INSTRUMENT UNDER TEST				TESTING INSTRUMENT (271C)			
STEP	APS TEST SETTINGS			COUNT INTERVAL BITS SW	DISPLAY		
	SEQUENCE SWITCH	RANGE SWITCH	STD/51A SWITCH		MIN.	NOM.	MAX.
1.	START	$X10^{-3}$	STD	10^6	0	0	0
2.	NO TR	$X10^{-3}$	STD	10^6	500	520	550
3.	NO TR	$X10^{-4}$	STD	10^6	50	52	55
4.	NO TR	$X10^{-5}$	STD	10^7	50	52	55
5.	NO TR	$X10^{-6}$	STD	10^8	50	52	55
6.	NO TR	$X10^{-7}$	STD	10^9	50	52	55
7.	TR	$X10^{-4}$	STD	10^6	200	210	220
8.	NO RST	$X10^{-4}$	STD	10^6	50	52	55
9.	RST	$X10^{-4}$	STD	10^7	30	33	36
10.	START	$X10^{-4}$	51A	10^6	0	0	0
11.	NO TR	$X10^{-4}$	51A	10^6	50	52	55
12.	TR	$X10^{-4}$	51A	10^6	200	210	220
13.	NO RST	$X10^{-4}$	51A	10^6	125	130	135
14.	RST	$X10^{-4}$	51A	10^6	50	52	55

3.0 OPERATION AND APPLICATIONS

3.1 Controls, Indicators, and Connectors

3.1.1 DS1/DS1C INPUT: Two, parallelled connectors; have one of which accepts a WE 310-type plug and the other a mini 310 plug. Insertion of a plug into either of these jacks interrupts the Test Set internal loop back and passes data from the system under test to the 273's receiver. Only one input jack at a time should be used.

3.1.2 DS1/DS1C OUTPUT: Six jacks, four of which accept WE 310-type plugs and two accepting mini 310 plugs. The four WE 310-type jacks provide four mutually independant outputs. Each of the mini 310 jacks is wired in parallel with an adjacent WE-310 jack. Only one jack should be connected to an adjacent pair at one time to preserve output impedance. The output impedance of all six jacks is 100 ohms ± 5%.

3.1.3 TERM/ALBO/BRIDGE: A three position toggle switch which determines the input circuitry and terminating impedance of the DS1/DS1C input. In the TERM position the input impedance is 100 ohms ± 5%. In ALBO position the input impedance is > 1000 ohms and is always treated as the complex line impedance provided by a 4000 ft. line. In the BRIDGE position the input is > 1000 ohms.

3.1.4 AUXILIARY INPUT/OUTPUT CONNECTORS: Four pin jacks and three BNC connectors plus a ground post (GND) are provided:

(a) TRANSMITTER BIT SYNC (Output): Generator clock output; 1.544 MHz for T1 and 3.152 MHz, for T1C. Bipolar square wave.

(b) TRANSMITTER WORD SYNC (Output): A pulse, 324 nsec for T1 and 160 nsec for T1C; generated once per full cycle of the Transmitter Pseudorandom sequence generator. Output level changed from high to ground for the duration of the pattern sequence.

(c) RECEIVER BIT SYNC (Output): The clock signal as extracted from incoming data by the Receiver clock extractor circuit.

(d) RECEIVER WORD SYNC (Output): A pulse, 324 nsec for T1 and 160 nsec for T1C; generated once per full cycle of the Receiver sequence generator; the output transition is from high to ground only for the duration of the pattern sequence.

(e) ERRORS (Output): A pulse, negative going pulse 324 nsec long for T1 or 160 nsec long for T1C; the output transition is from high to ground only for its duration.

(f) BLOCK ERRORS (Output): A pulse, 324 nsec for T1 and 160 nsec for T1C; for every error detected by the Receiver and processed in accordance with the error format selected by the DISPLAY FORMAT switch. The output transition is from high to ground only for its duration.

(g) EXTERNAL CLOCK: This input accepts a 3 ± 1 Volt ALL 1's bipolar signal. When connected, this signal automatically becomes the Transmitters reference clock which permits the 273 to operate synchronously with the T-Carrier equipment under test.

3.1.5 DISPLAY FORMAT: A four position switch which selects the type of error which will be registered on the Display.

(a) INDIVIDUAL: Every error detected by the receiver is counted and registered on the Display.

(b) ERRORED-SEC (Asynchronous): The data stream is divided into consecutive one second blocks. One or more errors detected in a block are counted as a single error. Error free seconds, asynchronous, may be determined by subtracting total block errors from the time of the test in seconds.

(c) ERROR-SEC (Synchronous): Occurrence of an error triggers a 1 second count. One or more errors during this period are counted as a single error. The next count does not resume until the occurrence of another error. Error free seconds, synchronous, may be determined by subtracting total errored blocks from the time of the test in seconds.

(d) 0.3 MS BLOCK: The Display counter is blanked for a period of 0.3 MS after an error is detected. The first error is added to the displayed count while errors following within the next 0.3 MS are ignored.

3.1.6 MODE Switch: A 3-position toggle switch used as follows:

(a) VIOLATIONS (up position): Conditions the Test Set for bipolar violation measurements. The Transmitter inserts bipolar violations in the quasi-random test sequence under control of the Self Test switch (3.1.9(c)) and the Receiver is set to count bipolar violations.

(b) APS (center position): Connects the output of the Receiver section to the input of the Transmitter section; an incoming signal plugged into the receive input jack is cleansed at bipolar violations permitting violations to be inserted into the Receiver data pattern at a rate selected by the APS TEST, RANGE and SEQUENCE switches.

(c) LOGIC (down position): Conditions the Test Set for logic errors measurements. The Transmitter inserts logic errors in the quasi-random test sequence under control when the Receiver is set to count logic errors.

3.1.7 (Bit Rate) SELECT: A two position switch that selects either a T1 (1.544 M bits/sec) or T1C (3.152 M bits/sec) Bit Rate in the DS1 or DS1C format, respectively.

3.1.8 SYNC mode Switch: a 2-position toggle switch used as follows:

(a) AUTO (up position): Sets the Test Set for automatic resynchronization at the QRSS pattern in the event synchronization is lost. The Lost Sync LED will provide a record that synchronization had been lost during the test period.

(b) MANUAL (down position): Resynchronization is initiated manually.

NOTE: The LOST SYNCHRONIZATION THRESHOLD is factory set for an error rate of twelve errors within fourty bits. Two other thresholds may be selected: 120 errors in 400 bits and 1200 errors in 4000 bits. Strap options for these thresholds are located on the RECEIVER LOGIC BOARD. Connecting straps across terminal pairs A1 and B1 selects the 120 bit error in 400 bit threshold. Connecting straps across pairs A1, B1, A2 and B2 selects the 1200 error in 4000 bit threshold.

3.1.9 SELF TEST Switch: A 3-position momentary toggle switch used as follows:

(a) NORMAL (center position): With no connection to the DS1/DS1C INPUT (Receiver), the Receiver and Transmitter are directly linked. If the MODE switch is set for LOGIC and the RESET/RESYNC switch is operated, all indicators will be off and the Display will show no count; if the MODE switch is set for VIOLATIONS, the NO SYNC and LOST SYNC indicators will be held ON as synchronization does not apply to measurement of bipolar violations.

(b) INTERRUPT DATA (momentary up position): Opens the link between Receiver and Transmitter, causing both the NO DATA and NO SYNC indicators to come on. Return to NORMAL position forces the NO DATA indicator OFF and LOST DATA ON. If the SYNC MODE switch is at AUTO, the LOST SYNC indicator will replace the NO SYNC upon return to NORMAL. The INTERRUPT DATA function is disabled when a plug is inserted into the DS1/DS1C INPUT jack.

(c) INSERT ERRORS (momentary down position): Depending on the MODE switch setting, inserts either logical errors or bipolar violations into the Transmitter test sequence. These errors appear at the DS1/DS1C OUTPUT (Transmitter) jacks and are directed to the Receiver input via internal loop back wiring if no plugs are inserted into the input and output jacks. In the Receiver, these errors exercise the detection and counter circuitry and are registered on the Display. Since a known quantity of errors is injected into the Receiver, this process provides a quick self-test. (See para. 2.2.5 thru 2.2.10). The INSERT ERRORS Switch must be held down to insert the full block of errors during the count interval.

The INSERT ERRORS position is also useful for line identification when the 273 is connected to T-Carrier equipment. When used in this fashion, all MODE switch positions will insert eight errors in 10^6 bits in the transmitted DS1/DS1C output (violation errors in APS or VIOLATIONS mode, data errors in LOGIC mode). In the APS position the RANGE and Sequence switches are disabled when the INSERT ERRORS switch is activated.

NOTE: The SELF TEST switch does not permit observation of the violation rates selected when the MODE switch is set to the APS position. An externally connected bipolar signal source and violation detector are required to determine proper operation. (Reference para. 2.2.30).

3.1.10 DISPLAY INTERVAL (SEC) Control: A variable potentiometer which determines the period of time the display will hold any given count; covers a range of from 1 to 10 seconds or continuous (HOLD).

3.1.11 RESET/RESYNC Switch: A free-return toggle switch that resets the Display counter, initiates a new count interval, resets the LOST SYNC indicator in LOGIC mode, resets the LOST DATA indicator and initiates resynchronization.

3.1.12 COUNT INTERVAL (Bits): A 6-position switch whose settings determine the bit interval that the counter circuits will use to count errors. Bit intervals are selected by the 10^6, 10^7, 10^8, 10^9, switch positions. The time base for these intervals is generated from the WORD SYNC signal. Therefore, the 10^6 bit position actually relates to 1,048,575 bits or approximately 10^6 (1,000,000 bits). Subsequent positions (10^7, 10^8, 10^9) are 10's multiples of 1,048,575.

(a) CONT: In this position the count will maintain continuously until reset by the RESET/RESYNC switch.

(b) TIMED: The count period is determined by the setting in minutes of the 3 timer thumbwheel switches.

3.1.13 TIMER: Three, ten position, thumbwheel switches which set a count interval between 0 and 999 minutes in one minute steps. A TIMER cycle is initiated with the momentary operation of the RESET/RESYNC switch. At the end of the TIMER cycle the final number registered on the Display is maintained until manually restarted by operation of the RESET/RESYNC switch.

3.1.14 TIMER STATUS: A 2-position free return toggle switch which when held in down position permits viewing on the Display of the "time remaining" in minutes in a TIMER cycle.

3.1.15 APS TEST Switches: A 5-position rotary switch (SEQUENCE) and a 5-position rotary switch (RANGE) control the insertion of bipolar violations when operating in the APS mode. The 2-position toggle switch (WECO/51A) further modifies the inserted violation rate (hysterisis) to effectively test either WECO standard or 51A Span line Switch equipment.

Violations uniformly spaced in time are inserted at the error rates listed in the Table Below:

SEQUENCE SWITCH	STD/51A SWITCH	BPV RATE RANGE SWITCH 10^{-3}	10^{-4}	10^{-5}	10^{-6}	10^{-7}
START	STD	0	0	0	0	0
NO TRANSFER	STD	$10^{-3.3}$	$10^{-4.3}$	$10^{-5.3}$	$10^{-6.5}$	$10^{-7.3}$
TRANSFER	STD	$10^{-2.7}$	$10^{-3.7}$	$10^{-4.7}$	$10^{-5.9}$	$10^{-6.7}$
NO RESTORE	STD	$10^{-3.3}$	$10^{-4.3}$	$10^{-5.3}$	$10^{-6.5}$	$10^{-7.3}$
RESTORE	STD	$10^{-4.5}$	$10^{-5.5}$	$10^{-6.5}$	$10^{-7.7}$	$10^{-8.5}$
START	51A	N/A	0	0	0	0
NO TRANSFER	51A	N/A	$10^{-4.3}$	$10^{-5.3}$	$10^{-6.3}$	$10^{-7.3}$
TRANSFER	51A	N/A	$10^{-3.7}$	$10^{-4.7}$	$10^{-5.7}$	$10^{-6.7}$
NO RESTORE	51A	N/A	$10^{-3.9}$	$10^{-4.9}$	$10^{-5.9}$	$10^{-6.9}$
RESTORE	51A	N/A	$10^{-4.3}$	$10^{-5.3}$	$10^{-6.3}$	$10^{-7.3}$

TABLE 3-1

NOTE: To avoid confusion to the operator, these rates are available only when the MODE switch is set to APS. However, some operators may find these rates useful when testing in the VIOLATIONS or LOGIC mode. It is possible to override this lock out feature by adding a strap to the terminal pair designated "A" located on the BUFFER/APS module (A7). If the strap is added, care should be taken to maintain the SEQUENCE switch in the START position when error (Logic/Violations) insertion is not desired.

3.1.16 DISPLAY: A 3-digit, seven segment, solid state indicator which presents a numerical readout of error count accumulated during any count interval.

3.1.7 OVERFLOW Indicator: A solid state indicator which is energized when the error count exceeds the numerical capacity of the Display (999).

3.1.18 COUNT Indicator: A solid state indicator which is energized during error count intervals.

3.1.19 RECEIVE STATUS Indicators: Six solid state indicators for the following purposes:

(a) NO DATA: Energized when data is not being presented to the receiver.

(b) LOST DATA: Energized after data has been lost and subsequently regained; remains on until the RESET/RESYNC switch is activated. This indicator, with the NO DATA indicator, thus provides coverage of data loss from the instant of stoppage to the instant of manual resynchronization.

(c) NO SYNC: Energized when the receiver is not synchronized to incoming QRSS data, or when the test set is in the VIOLATIONS or APS mode. Alerts the operator to measurement status of Test Set avoiding the use of bipolar violations for error measurements rather than logic errors for error measurements, when the network includes equipment which corrects or otherwise invalidates the use of bipolar violations for error measurements. See Para. 3.3.1(d).

(d) LOST SYNC: Energized when receiver synchronization with incoming QRSS data has been lost and subsequently recovered and remains on until the RESET/RESYNC switch is actuated. If the Test Set is in the VIOLATIONS or APS mode, LOST SYNC is held on.

(e) LOST POWER: Energized as the Test Set is first turned on and then when a power disturbance of sufficient magnitude to invalidate data is detected. In either case, it remains on until the RESET/RESYNC switch is actuated.

(f) ALL 1's: Energized after a consecutive string of 1024 1's have been detected. The detection of a zero immediately resets internal circuits. However, the indicator is maintained for 100 MS to assure visibility of minimal length ALL 1's patterns. Removing strap "A" of the A3 board will cause the ALL 1's to be detected after one hundred 1's have been detected (4.4.3.7).

3.1.20 POWER: The Test Set may be powered by either 117 VAC ± 10%, 47-63 Hz or negative 48 VDC ± 4 VDC. Each power supply is separately fused; spare fuses are located in the dust cover. The AC input is a recessed male connector which mates with one end of the Test Set's power cord. The DC power is applied to the rear of the Test Set through a WE-247 T-C type jack. Direct current powering is intended to be supplied from the 24V,

positive ground, Central Office battery. Battery -48 is applied to the plug tip (T), +48 (ground) to the sleeve. Power cords should be mated to the Test Set first, followed by the power source.

The Test Set is protected against simultaneous operation from AC & DC sources. However, this mode of power operation is not recommended.

3.2 PRINTER/REMOTE INTERFACE (Option P)

Listed in Table 3-3 are all of the signals appearing on the Interface Connector, their specific functions, and pertinent details of the interface circuitry within the Test Set itself. External connection to the Printer/Computer Interface Connector is made by using an Amphenol No. 57-30500 (or equivalent) connector.

3.2.1 Remote Control:

placing the front panel switches in their open-circuit positions and manipulating the control lines via the interface connector. The correct switch positions for remote control are listed in Table 3-2, and the functions of the control lines are listed in Table 3-3. All control lines are TTL compatible and may be interfaced with TTL driver circuits. RESET/RESYNC and Pin 15 must be driven by a buffer gate, contact closure, or transistor switch rather than by a standard TTL driver. This results from the requirement on the driver to sink 25 mA, which is equivalent to a fan-out of fifteen standard TTL loads.

Table 3-2: Remote Control Switch Position

Switch		Position
MODE:		
VIOLATIONS/ERRORS/APS	to	APS
APS TEST:		
SEQUENCE	to	START

When the Test Set is under remote control, a new test may begin, or a test in process may be aborted, by operating the RESET/RESYNC line. This is equivalent to operating the corresponding front panel switch. When resetting the Test Set, a ground should be applied to Pin 15 for a period of not less than 10 msec. A new test will automatically start within 0.7 sec of the time when pin 15 is again open-circuited. The start of the new test will be signified by the lighting of the COUNT indicator and a logical 0 appearing on pin 18 of the interface connector.

of the COUNT indicator on the front panel, the return of pin 18 to a logical 1, and the leading edge of the 100 msec print pulse on pin 38.

Table 3-3: Printer/ Computer Interface Connector - Signals and Pin Assignments

Pin No.	Signal ID	Signal Function	Interface
1	$10^0 - \bar{1}$	Units digit, BCD inverted, A bit	TTL output *
2	$10^0 - \bar{2}$	Units digit, BCD inverted, B bit	TTL output *
26	$10^0 - \bar{4}$	Units digit, BCD inverted, C bit	TTL output *
27	$10^0 - \bar{8}$	Units digit, BCD inverted, D bit	TTL output *
3	$10^1 - \bar{1}$	Tens digit, BCD inverted, A bit	TTL output *
4	$10^1 - \bar{2}$	Tens digit, BCD inverted, B bit	TTL output *
28	$10^1 - \bar{4}$	Tens digit, BCD inverted, C bit	TTL output *
29	$10^1 - \bar{8}$	Tens digit, BCD inverted, D bit	TTL output *
5	$10^2 - \bar{1}$	Hundreds digit, BCD inverted, A bit	TTL output *
6	$10^2 - \bar{2}$	Hundreds digit, BCD inverted, B bit	TTL output *
30	$10^2 - \bar{4}$	Hundreds digit, BCD inverted, C bit	TTL output *
31	$10^2 - \bar{8}$	Hundreds digit, BCD inverted, D bit	TTL output *
7	$\overline{\text{OVERFLOW}}$	Logical 0 when OVERFLOW indicator on	TTL output **
18	$\overline{\text{COUNT}}$	Logical 0 when COUNT indicator on	TTL output **
35	$\overline{\text{NO DATA}}$	Logical 0 when NO DATA indicator on	TTL output **
8	$\overline{\text{NO SYNC}}$	Logical 0 when NO SYNC indicator on	TTL output **
9	$\overline{\text{LOST POWER}}$	Logical 0 when LOST POWER indicator on	TTL output **
10	$\overline{\text{ALL 1's}}$	Logical 0 when ALL 1's indicator on	TTL output **
15	RESET/RESYNC	Ground to Reset Test Set	Switch, 15 TTLS inputs 10K ohm to +5V

*See Para. 3.2.2
**See Para. 3.2.3

Table 3-[illegible]: Printer /Computer Interface Connector - Signals and Pin Assignments (cont)

Pin No.	Signal ID	Signal Function	Interface
45	VIOLATIONS/APS	Ground or logical 0 for violations both 45 and 44 open or logical 1 for APS	4 TTLS inputs 2K to +5V
44	ERRORS	Ground or logical '0' for Errors	4 TTLS inputs 2K to +5
16	$\overline{\text{NO TR}}$	Ground or logical '0'	1 TTLS input 10K to +5
41	$\overline{\text{TR}}$	Ground or logical '0'	1 TTLS input 10K to +5
17	$\overline{\text{NO RST}}$	Ground or logical '0'	1 TTLS input 10K to +5
40	$\overline{\text{RST}}$	Ground or logical '0'	1 TTLS input 10K to +5
	START	Pins 16, 17, 40, 41 at +5 or logical '1'	
46	EXT. ERRORS	For each negative transition of a clock signal one error will be inserted into the transmitted data.	1 TTLS input, 10K to +5
47	$\overline{\text{ZERO SUPPRESS}}$	Ground or logical '0' will convert the T1C quasi-random pattern from nineteen consecutive zero format to a restricted fourteen consecutive zero format.	1 TTLS input 10K to +5
[illegible]	$\overline{\text{ERROR STRAP}}$	Ground or logical zero will permit APS error rates (SEQUENCE, RANGE, 51A/STD switches) to be used in VIOLATIONS and LOGIC modes in addition to APS.	1 TTLS input 10K to +5V
21	[illegible]	Ground or logical '0' to insert 8 errors per 10^6 bits	3 TTLS inputs 2K to +5V
[illegible]	[illegible]	Normally high, pulls to ground for 324 nsec every 1,048,575 bits	Transistor sw to gnd, 75 ohm to +5V
[illegible]	[illegible]	Chassis ground and signal return	
[illegible]	[illegible]	+5V output for reference only ($<$ 50 mA)	

Table 3-3: Printer/Computer Interface Connector - Signals and Pin Assignments (Cont)

Pin No.	Signal ID	Signal Function	Interface
37	CARRY	Normally low, goes to logical '1' for 10 msec when 3-digit error counter overflows	TTL output
38	PRINT	Normally low, goes to logical '1' for 100 msec at end of count interval	TTL output
43	ALL 1's PATTERN	Ground or logical '0', Test Sets DS1/DS1C output pattern is converted to bipolar all 1's	1 TTLS input 10K to +5

3.2.2 BINARY-CODED DECIMAL (BCD): The three decimal digits of the internal error counter and display are brought out on twelve interface lines. The information is presented in 1248, BCD code and all twelve outputs are in the inverted sense. These signals are buffered by TTL inverters located on the BUFFER/APS Module of the Test Set for the purpose of protecting the internal circuitry; therefore, these lines are capable of sinking 8 mA and sourcing 200 uA, which is equivalent to ten standard TTLS loads. Care should be taken to avoid conditions which exceed these current levels or cause the voltage applied externally to go beyond the range of 0 to +5 V dc.

3.2.3 INDICATOR LIGHTS: The information presented on six of the eight Receive status indicators is duplicated in these six signals. The information is presented such that a low level or logical zero is presented when the corresponding indicator is lighted. Like the BCD lines above, these are buffered by TTL inverters in the BUFFER/APS Module of the Test Set.

3.2.4 CONTROL: These interface lines provide parallel access to the major front panel switches of the Test Set. They may, therefore, serve as outputs for monitoring switch settings or as inputs for remote control of the Test Set. If the front panel switches are set as listed in Table 3-2 +5 V will appear on all input lines and remote control may be affected via contact closures or NPN open-collector switching to ground.

These input lines are connected directly to one or more TTL inputs without input buffering (ref. Figure 3-1). The front panel switch to ground and 10K ohms resistors to the +5 V supply are also connected to these inputs. Any device driving these inputs must be capable of sinking current equal to 1 mA plus 0.8 mA times the number of TTL inputs indicated in Table 3-3. Since the 10K ohm resistive pull-up is provided internally

and the control lines may be shorted to ground by the front panel switch, the driving device should not be capable of sourcing current. The voltage of the inputs, including transients, must be restricted to between ground and the internal supply, as provided on pin 36 of the Interface Connector.

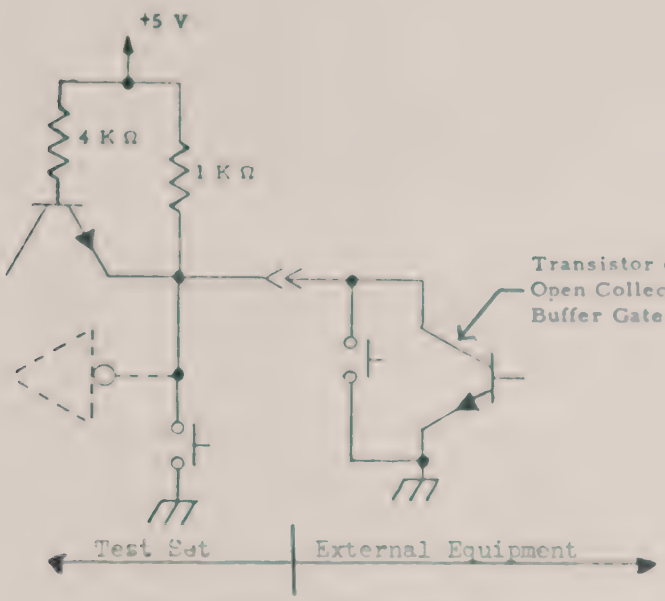


Figure 3-1: TTL Inputs

3.2.5 +5 V DC: The internal logic supply of the Test Set is provided on pin 36 of the Interface Connector for reference purposes. It should be used by the external interface circuitry to signify the maximum external voltage that can be tolerated at most of the TTL inputs and outputs. This includes the possibility in which the external circuitry is powered and the Test Set is not powered, or vice versa. The internal supply and pin 36 are separated by a 1 K, 1/4 W resistor (R38). If it is necessary to by pass this resistor, caution should be exercised not to exceed a maximum current of 50 mA.

3.2.6 PRINT AND CARRY OUTPUTS: The carry output generates a 10 msec pulse each time the 3-digit display of the Test Set overflows. The 100 msec print pulse is generated at the end of each count interval when the COUNT indicator is extinguished. Both outputs are derived from TTL devices and normally remain low.

3.2.7 [illegible]: The auxiliary output is derived from TTL transistor switches with 75 ohm pull-up resistors to the +5 V supply. The transistors should not be required to sink more than 30 mA of current through the Interface Connector and the voltages must be restricted to between ground and +5 V. These outputs may be shorted to each other or to ground without danger of damage to the internal circuitry.

3.3 Applications

The Bowmar Model 273 Digital Carrier Analysis Test Set can be used to test any Digital Transmission System or component accepting a T1 (DS1, 1.544 mbs) or T1C (DS1C, 3.152 mbs) bipolar signal. This Test Set performs bipolar violation and logical error measurements. Bipolar violations are defined as transmission format errors where two or more "1"s are transmitted with the same polarity, consecutively irrespective of zero content. Logical errors occur when a data bit is mistakenly converted from a "1" to a "0" or a "0" to a "1" by a malfunction or noise within the communications system. Logical error detection requires that the information content of the data being transmitted is known. The Bowmar 273 contains a quasi-random signal source (QRSS) identical to the Western Electric J98710R T1 QRSS. This test source provides the Data Base used in logical error measurements and presents a realistic stress on the equipment under test.

The Bowmar Model 273 may be used to test: T1 and T1C Carrier Systems; Digital Radio Systems; GTE Duo Binary Systems; AT&T Digital Data Systems (DDS); APS Tests on T1 Outstate, DDS, TSPS, or any system using Automatic Span Line Protection switches; Multiplexers such as M12 and M1C.

This Applications Section is not intended to give the operator a detailed set of steps to follow. Rather the intent of this Section is to acquaint the operator with a wide variety of test schemes and general methods. For specific details consult the appropriate System Practice.

3.3.1 Operation:

(a) (BIT RATE) SELECT Switch (T1/T1C)
This control selects either T1 (DS1, 1.544 mbs) or T1C (DS1C, 3.152 mbps) data transmission rates. The data rate chosen must agree with that of the system under test.

(b) Monitor Jacks and Cross Connect Points
The Receiver of the Test Set can be made to either bridge or terminate the line which is connected to the DS1/DS1C input 310 jack. The TERM/ALBO/BRIDGE switch makes this selection. In the TERM position the Receiver presents an impedance of 100 ohms ± 5% while the ALBO and BRIDGE positions represent more than 1000 ohms.

When using the ALBO input to measure BER at distances ranging from 500' to 4000' from the repeater, the line must be terminated either by operating equipment or a 100 ohm ± 5% resistor.

At Cross Connector Monitor points the TERM (100 ohm) position should be selected to provide the proper line terminating impedance. The DSX Patch Bay Monitor jacks are designed with isolation resistors to prevent double line termination when using test instruments with a 100 ohm input.

The TERM/ALBO/BRIDGE switch determines the Receive DS1/DS1C input impedance only. The DS1/DS1C transmitter outputs have a constant source impedance of 100 ohms ± 5%.

(c) Receiver Status Indicators
In the VIOLATIONS or APS test mode, both the NO SYNC and LOST SYNC indicators are held "ON", and are not to be considered a test failure. These indicators are held on to remind the operator that the set is conditioned to measure bipolar violations (See Para. d). Maintaining these indicators ON ensures functional compatibility with AT&T Technology KS-20775 L1 and L2 specifications and other Bowmar Test sets.

Synchronization of the Receiver can only be achieved if the received data is a QRSS (Logic) pattern identical to Western Electric J98710R, or the output of Bowmar Model 273 or 271 Test Sets. Since bipolar violation testing is indpendent of the data content, synchronizing is neither necessary or possible when the mode switch is either in the VIOLATIONS or APS position.

(d) Violations Test
Some T-Carrier equipment (e.g. multiplexers) remove bipolar violations. It is, therefore, possible when inserting violations into the test pattern that no violations, or something other than that anticipated, may be detected at the far end station.

(e) Errors, Block Errors, and EXT. Clock

1. Errors/Block Errors - These two BNC connections are outputs which may be connected to an external counter or the Model 273B-B cover option. The errors connection presents a Hi (+5V) to Low (Gnd) transition for every error detected by the Test Set regardless of the position of the DISPLAY FORMAT switch. It can be used when the Test Set's three digit display is not large enough or when a simultaneous count of individual errors and formatted errors (Errored Seconds (Async), Error Seconds (Sync); or error counts with 0.3 MS blanking) is desired.

   The Block errors output presents a Hi to Low transition for errors detected and formatted in accordance with the position selected by the DISPLAY FORMAT switch.

2. EXT. Clock - This input permits the Test Set's transmitter to be synchronized with the communications system equipment under test or associated equipment such as a Jitter Generator. The input requires a 3V ± 1V bipolar ALL 1's pattern.

3.3.2 General Test Preparation

(a) Check for the presence of the proper fuse.

1. AC line operation, 3AG, 1/2A, Slo Blo, located on front panel.

2. DC, 48V central office battery operation, 3AG, 3/4A, Slo Blo, located at rear of outer case.

NOTE: Spare fuses located in cover.

(b) Connect the power cord between the Test Set and a suitable power outlet.

1. AC power, 115 VAC ± 15%, 47 - 63 Hz, Single Phase.

2. DC power, -48 VDC ± 4 V, positive bat. ground, connected through a WE247 jack, tip to -48 VDC, positive ground to sleeve.

CAUTION: Power cords should be connected to the Test Set first followed by connection to the power source.

(c) Set Power switch to ON.

(d) Set the (BIT RATE) SELECT switch (T1/T1C) to correspond with the system under test.

(e) Connect a patch cord between the Test Set's DS1/DS1C input to either a monitor or cross connect jack.

Set the TERM/ALBO/BRIDGE switch to TERM for all DSX MONITOR connections at cross connect jacks.

(f) Set the DISPLAY INTERVAL control for comfortable display viewing, between 1 and 10 seconds or hold.

(g) The ERROR FORMAT switch should generally be set to INDIVIDUAL such that all errors detected are displayed. Certain tests and conditions where large error bursts can be expected will require use of the other error (DISPLAY FORMAT switch) positions.

(h) The COUNT INTERVAL (BITS) control setting is dependent on the expected or actual system error rate.

NOTE: A count of 10 on the Display and a switch setting of 10^8 equates to an error rate of less than 10^{-7}. This mathematical manipulation is true of all switch position/display counts combinations.

(i) The SYNC MODE switch should generally be set to AUTO. This switch is applicable to logical error measurements only.

(j) Operate the RESET/RESYNC switch. This starts a new test interval. The count registered on the DISPLAY when the COUNT indicator is OFF, in conjunction with the COUNT INTERVAL chosen, determines the error rate.

(k) Line Identification. A through transmission path can be verified by using the Test Set's ability to insert errors into its transmitted QRSS data pattern. Holding the SELF TEST switch in the INSERT ERROR position injects 8 errors per 10^6 bits, 80 per 10^7, etc. Detection of this error rate at the far end verifies a through transmission path. Caution should be exercised for this verification procedure to use the LOGIC measurement mode as some communications equipment (e.g. Multiplexers) remove bipolar violations.

(l) Other control settings depend on the type of tests to be conducted.

3.3.2 System Tests

3.3.2.1 End-To-End Error Rate Measurements

The Test Set's Receiver and Error Detection Circuits are utilized in end-to-end testing. The Test Set is connected to either a MONITOR or CROSS CONNECT jack. Data is placed on the Line/System under test at the far end using either a Western Electric J98710R quasi-random signal source, a second Bowmar Model 273 or a Bowmar Model 271A, B, C (KS-20775 L1, L2). Either LOGICAL ERROR or VIOLATIONS measurements can be made.

3.3.2.2 Loop Back Error Rate Measurements

Loop Back tests require the far end to be patched back to back. The Transmitter (DS1/DS1C output) of the Test Set is connected to the line at the near end, supplying a quasi-random signal source. The Test Set's Receiver is connected to either a monitor or cross connect access jack. Either VIOLATION or LOGICAL ERROR measurements may be made.

3.3.2.3 Monitor In-Service Bipolar Violations

Bipolar Violations may be measured at any time on an in-service line without disturbing that line. The 273's DS1/DS1C input is connected to a MONITOR jack. The TERM/ALBO/BRIDGE switch must be in the TERM position at a DSX Patch Bay or in BRIDGE when connected directly across a line or a distributing frame.

3.3.2.4 Multiplexer Tests

Multiplexers, such as M12 and M1C, may be tested by looping the multiplexer back on itself and applying a test signal to its inputs. The 273 provides up to four independent DS1/DS1C outputs which may be connected to a multiplexers input ports. Connecting the Test Set's DS1/DS1C input to each of the multiplexer's output ports completes the test data path. Multiplexers remove bipolar violations, therefore, logical error testing should be performed.

3.3.2.5 Automatic Span Line Protection Switch (APS) Tests

At present, systems such as T1 outstate, DDS, and TSPS utilize Automatic Span Line Protection Switches (APS). The majority of switches in use may be classified as two types. The first follows the specifications outlined by AT&T Bell Laboratories which refers to a hysterisis switch, referred to by Bowmar as STANDARD (STD). The second type was developed prior to Bell Labs' initial specification and is referred to by Bowmar as 51A. The wide acceptance of the 51A equipment by the operating companies has resulted in Bell Labs' recognition with appropriate specification standards.

The 273 is connected to an in-service line such that it is in series with the data path for one direction of communication. The 273's MODE switch is set for APS and TERM/ALBO/BRIDGE switch to TERM. A cable is connected between the 273's input and a monitor jack in the system under test. A load plug is inserted into the corresponding output jack of the system under test to preserve line impedance and one of the 273's four DS1/DS1C outputs is connected to the Cross Connect input jack. The 273's APS [illegible] signal is set to match the Test Set as the Type Line Switch [10^4, 10^5, 10^6, 10^7, (10^3 available for STD only)]. The setting of the STD/51A switch should correspond to the type of equipment being tested.

Set the SEQUENCE Switch to START and observe that the alarm indicators on the Span Line Switch equipment show the line to be tested as, in-service. Set the SEQUENCE Switch to NO TR (NO TRANSFER). Equipment alarms should show that the line under test remains in service. Place the SEQUENCE Switch to TR (TRANSFER). Alarm indicators should identify the line under test as failed and data switched to the stand by line. Rotate the SEQUENCE switch to NO RST (NO RESTORE). The alarm status for TR should hold. Set the SEQUENCE Switch to RST (RESTORE). Normal service should return to the line under test.

4.0 THEORY OF OPERATION

General

Refer to the Block Diagram (Figures 4-1 and 4-2) and the Schematics of Section 6 to correlate descriptions offered in this section.

4.1 Transmitter

The Transmitter section of the Digital Carrier Analysis Test Set is a DS1/DS1C (T1, T1C) type test source. The data base for the transmitted signal is provided by either a continuously repeating Quasi-Random sequence identical to that provided by Bell System Test Sources (e.g. WE J98710R, T1 Signal Source), or as selection of three repeating patterns including All Ones, 1-0-1-0 and 1-1-0-0. The transmitter is also capable of inserting errors (bipolar violations or logical bit errors) into the transmitted data base. When operating in the APS mode, the transmitted data is equal to that received from the system under test.

The T1 (DS1) transmitter output is a 1,544 mbps, 3 volt, bipolar, return-to-zero signal with trailing edge overshoot. The Quasi-Random signal source provides a 1,048,575 bit repeating pattern limited to fourteen consecutive zeros.

The T1C (DS1C) transmitter output is a 3,152 mbps, 3 volt, bipolar, return-to-zero signal. The Quasi-Random signal source provides a 1,048,575 bit repeating pattern with up to nineteen consecutive zeros.

Controlled error insertion makes it possible to provide this Test Set with a self test feature, line identification, and span line automatic protection switch (APS) testing. When the DS1/DS1C input is removed, the Test Sets' Transmitter is automatically looped back to the Receiver by an internal relay. Operating the SELF TEST switch to insert errors instructs the Transmitter to insert four pairs of errors every complete cycle of the Transmitter's sequence generator. These errors will be detected by the Receiver and displayed, providing a method of self test. When testing T-Carrier Systems it is possible to confirm a data path, end-end or loopback connection, by inserting this error pattern and monitoring for its presence at the terminating station.

The Quasi-Random sequence generator provides four patterns of seventeen or more consecutive zeros each cycle. A pair of errors is inserted each time one of these patterns is detected, thereby producing a fixed error rate of eight errors per cycle, (1,048,575 bits).

Logical error insertions of a zero-to-one and a one-to-zero conversion are performed by altering the function of the circuit which limits the output sequence to a maximum of fourteen consecutive zeros. This alteration is accomplished without violating either the fourteen-zero restraint (T1) or the bipolar format.

Bipolar violations consist of four consecutive ones, the first two of one polarity, and the second two of opposite polarity. This is accomplished by inhibiting the Bipolar Generator which normally alternates the polarity of each consecutive one, whether or not they are interspersed with zeros.

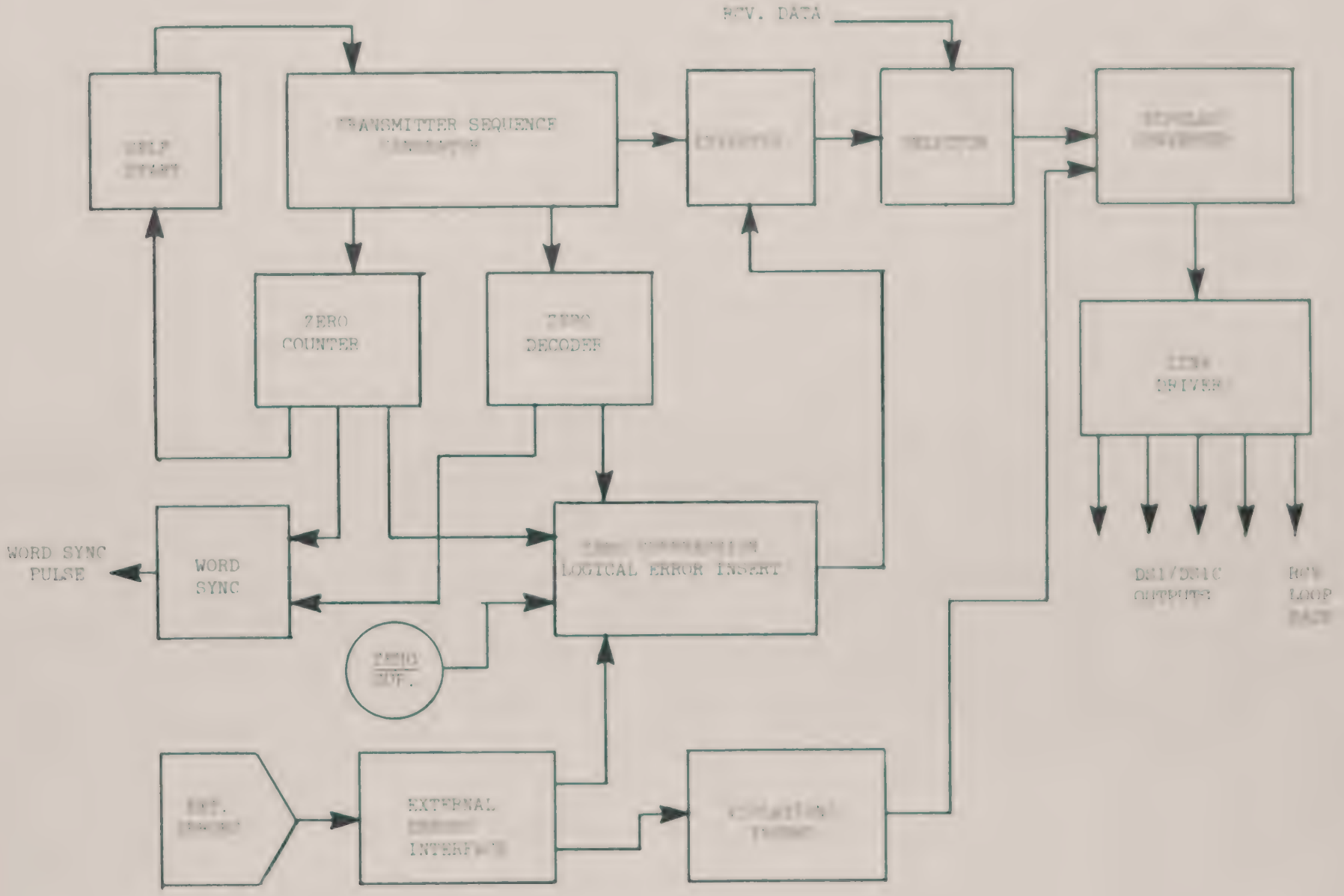
The Chart below illustrates a typical condition of eighteen zeros in the Sequence Generator. Note that the first four zeros when operating at the T1 rate have been converted to 1's to satisfy the 14 zero constraint. This Chart defines the format used for 14 zero limiting and error insertion.

Description		Data Stream Segment
Any condition of 17 or more zeros (18 shown) in Sig. Gen. output:	1st out	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
Corrected output (without errors):	T1	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
	T1C	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
Corresponding Xmitter output, Bipolar Format:	T1	+ - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 - + -
	T1C	+ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 - + -
Gen. output with Logical Errors:	T1	0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
	T1C	0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1
Corresponding Xmitter output, Bipolar Format:	T1	0 + - + - + 0 0 0 0 0 0 0 0 0 0 0 0 0 - + -
Errors:		X X
Bipolar Format:	T1C	0 0 0 0 0 + 0 0 0 0 0 0 0 0 0 0 0 0 0 - + -
Corrected Xmitter output with Bipolar Violations:	T1	+ + - - + 0 0 0 0 0 0 0 0 0 0 0 0 0 - + -
Violations:		X X
Bipolar Violations:	T1C	+ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 + - -
Violations:		X X

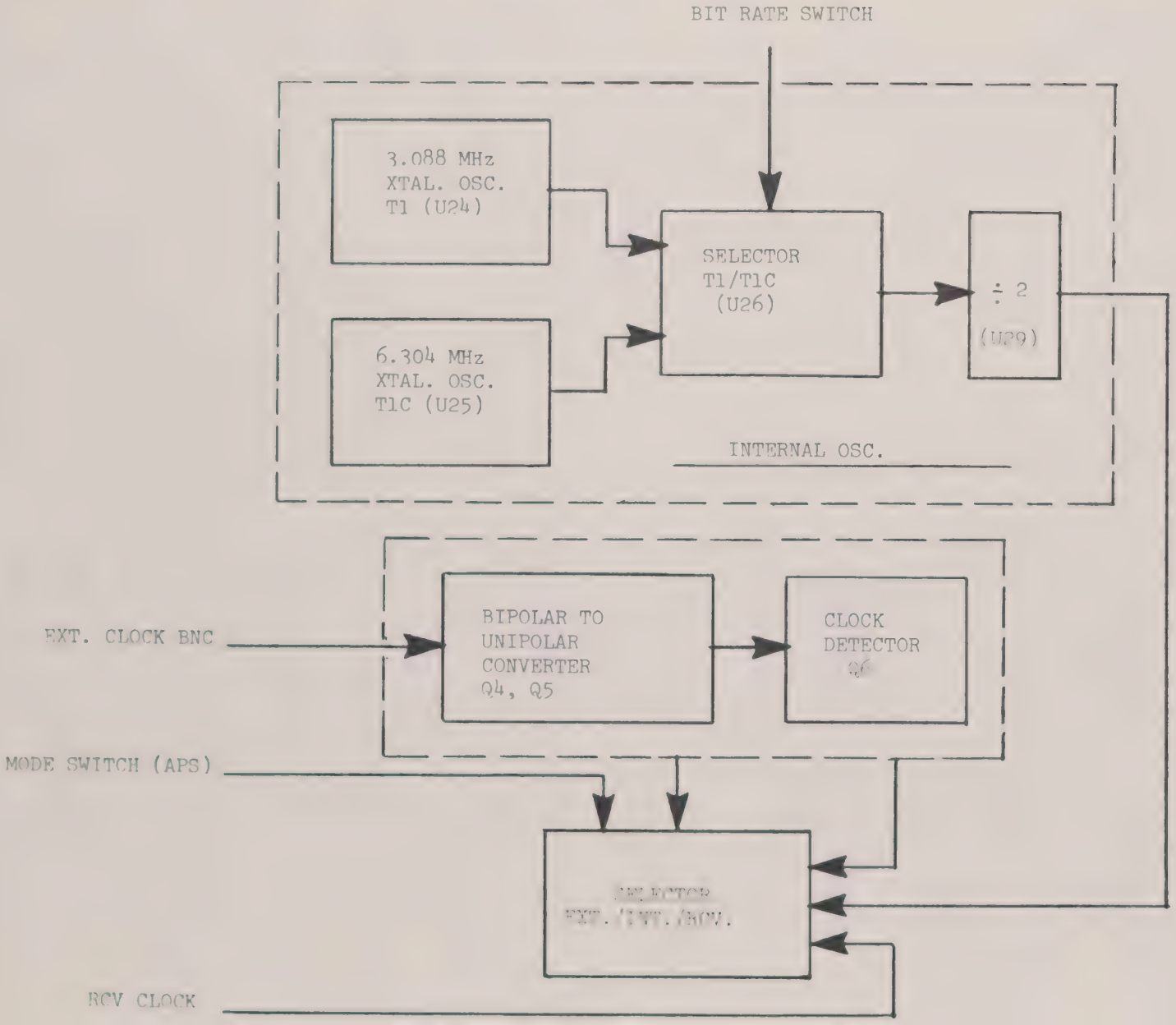
The rate at which violations are inserted by the APS circuits is determined by an independant oscillator and programable divider circuit. The APS RANGE and SEQUENCE switches define the clock rate exiting the divider circuit. Each complete clock cycle introduces one violation in the transmitted output.

The Transmitter Error Insertion circuits can be activated by an external signal applied to the Printer INTERFACE connector Pin 46 (option). A single Error, Violation or Logical as determined by the MODE switch, will be inserted into the transmitted output for each negative transition of the EXT. ERROR clock source.

TRANSMITTER BLOCK DIAGRAM FIG. 4-1A



TRANSMITTER BLOCK DIAGRAM FIG. 4-1B



4.2 Receiver

In the TERM and BRIDGE positions of the Input Select Switch, incoming data, in Bipolar format, is processed by a Receiver with slicing threshold proportional to the peak of the received signal. In the ALBO position, the incoming data in Bipolar format is processed by an AUTOMATIC LINE BUILDOUT circuit to remove amplitude and phase delay degradation imposed by cable characteristics. A slicer converts the processed received signal to a pulse format required ty TTL logic.

When the content of the received data is such that it contains only 1's data, an all 1's indication is established. A pattern of 1024 consecutive 1's must be detected. (See Para. 3.1.19(f)).

Reshaped data, after sampling, is directed to the Bipolar Violations Detector and the Bipolar/Unipolar converter.

The first circuit looks for two consecutive 1's of the same polarity, while the second circuit converts data from Bipolar to unipolar format. The outputs of these two circuits are then AXDed. If the mode switch is set for VIOLATIONS, the received data, in unipolar format, is routed to the Receiver Sequence Generator. This Generator differs from its Transmitter counterpart only in its monitor points and in a modified feedback loop; otherwise, it is capable of the same 1,048,575 bit test patterns. Its purpose is to provide a test pattern for checking the incoming unipolar data for logical errors by a process described in later paragraphs.

If the mode switch is set for VIOLATIONS, unipolar data is ignored, and the output of the Bipolar Violations Detector is forwarded directly to the Error Format Circuits, Counter and Display. In this situation, the Receiver Sequence Generator is made to continuously cycle simply to provide a time base for test length selection via the ERROR INTERVAL [sic] switch. When operating in this capacity, the Sequence Generator is self-starting, but it does not attempt to synchronize to the unipolar data stream.

and the Sequence Generator loop is closed, and the Generator output becomes its own natural pattern. The incoming unipolar data is then compared with this output and checked for logical error content. Logical errors are fowarded to the error format circuits, counted and displayed.

The DISPLAY FORMAT switch determines the type of weighting (individual, errored second, error second, 0.3 ms blank) which is applied to the detected errors (logic or violations) before being displayed. The effects of the DISPLAY FORMAT Circuit are described in Section 3.1.5.

Test duration is determined by the COUNT INTERVAL Control. The Display registers errors per one, ten, one hundred or one thousand cycles of the Receiver Sequence Generator by selection of the 10^6, 10^7, 10^8 or 10^9 positions respectively of the COUNT INTERVAL (BITS) switch. CONT or TIMER positions are used for MANUAL mode operation or for very long time intervals.

When operating in the APS mode, violations are introduced into the data by the APS Violations Control Generator. Received data is forwarded directly to the Transmitter from the Bipolar/Unipolar converter. The APS Violations Control determines the rate at which Bipolar violations will be introduced into the received data by the Transmitter's Bipolar Converter. In this mode, the Test Set acts as a repeater by re-transmitting data which it has received from equipment under test. The APS RANGE, SEQUENCE and STD/51A switches determine the violation rate introduced.

4.3 TRANSMITTER CIRCUITS (A4 MODULE)

4.3.1 Internal Oscillator

Either of two crystal oscillator circuits (U24, U25) are selected by steering logic (U26) and divided by a single flip-flop (U29).

The flip-flop output provides a symmetrical clock at either 1.544 MHz (T1) or 3.152 MHz (T1C) as selected by the (BIT RATE) SELECT (T1/T1C) switch.

The crystal oscillator operates in series mode with two, tandem connected, TTL inverters providing the necessary positive feedback path. A third inverter in conjunction with resistors R34 or R33 determine the crystal drive current. Adjustable capacitors C14 and C18 are frequency trims for the 3.088 MHz and 6.304 MHz crystals respectively.

4.3.2 External Clock

The external clock circuit converts (Q4, Q5) a 3 ± 1 V Bipolar, all 1's, signal to a square wave for use as the Transmitter clock. A detector [illegible] Selector, which automatically switches from Internal to External clock.

The secondaries of transformer T2 present an inverted and non-inverted, [illegible] respectively. Transistor Q4 conducts only for negative pulses of the external clock with Q5 conducting for positive pulses. The collectors of Q4 and Q5 are connected together to form a wired-or output.

Transistor base resistor/capacitor (R35/C21, R36/C22) networks reduce the effects of base storage to improve switching speed. Resistors R45 and R46 determine the circuit input impedance.

The converted square wave at the collectors of Q4 and Q5 is inverted and passed to the Detector Circuit (Q6). With no external clock, the transistors Q4 and Q5 are cut off. Transistor Q6 is off and capacitor C23 is charged to +5 volts through R43.

When the external clock is present, Q6 is switched at the clock rate [illegible] the INT/EXT/RCV Selector to select the external clock.

4.3.3 Selector INT/EXT/RCV

[illegible] external clock or receiver clock will control the transmitter circuits. The external clock detector signal is the dominant control followed by the APS position of the MODE switch. In the APS MODE the Transmitter is controlled by the receiver clock.

4.3.4 Sequence Generator

[illegible] with feedback directed through the exclusive-OR circuit of U5A.

The Sequence Generator provides a continuously repeating sequence of 1's and 0's. Each sequence is made up of all but one of the 2^{20} possible combinations of 20-bit states, for a total of 1,048,575 bits. The one exception is the all-zero state in which the Generator, by nature of its circuitry, will not function. In a situation where all-zeros might occur, a Self Start circuit (Ref. 4.3.6) is available to respond with injection of a 1 to unlock the Generator. During normal operation, the maximum count of 0's in the Genrator is nineteen.

The main output of the Generator is taken from the 20th stage. Auxiliary outputs from the 2nd, 3rd, and 4th stages enable monitoring of the serial progression of bits through Generator stages for purposes of determining self start, zero suppression, error insertion, etc. Each generated bit shifts a stage at a time with each Clock pulse.

Since auxiliary outputs are several stages ahead of the main output, they offer a preview of the output sequence of bits. This feature permits the necessary advance notice required for such actions as the fourteen-zero constraint, or the seventeen or more 0's state for error insertions, etc.

A four to one multiplex U30 selects one of the four data patterns - quasi-random, 1010, 1100, ALL 1's. The selection is from the front panel switches through Pin R & Pin S to this module.

4.3.5 Zero Counter

A zero counter monitors the number of zeros passing stage four of the sequence generator. The counter is actually incremented by clock pulses, but is reset by registration of a 1 so that the accumulated counts represent a series of 0's.

The Binary counter U8 is preset with a count of 1. After the passage of 15 consecutive zeros U8 sets flip-flop U11a. One half clock period later U11b is set. The outputs from these flip-flops control zero suppression and error insertion logic.

4.3.6 Self Start

Self starting is initiated through a single gate (U7A) by a count of twenty from the Zero Counter. This count is possible only if the sequence Generator is locked into the all-zero state and Clock pulses continue to increment the Zero Counter. The only opportunity for all-zero lock-up and self starting occurs when the Error Rate Test Set is switched on for use

As described earlier, the Sequence Generator cannot function in an all-zero state, therefore, upon registration of twenty 0's by the zero Counter, the Self Start circuit is activated to force a 1 into the input of the 1st stage of the generator. This resets the Counter and stimulates the Generator into normal operation.

4.3.7 Zero Detector

The zero Detector (U9B, C, U10) working in conjunction with the Zero Counter identifies patterns of seventeen or more consecutive zeros in the Sequence Generator. A NAND gate U9B looks at the sequence Generator two outputs earlier than the Zero Counter. This two bit look ahead combined with the fifteen zero detection of the Zero Counter is latched by flip-flop U10. Outputs from this detector control error insertion and Transmitter Word Sync.

4.3.8 Word Sync

A single gate (U9A) with inverter (U9C) makes up the Word Sync circuit. This state combines a count of seventeen from the Zero Counter and a two bit look ahead from the Zero Detector. The combination produces a pulse for each pattern of nineteen zeros which occures only once every 1,048,575 bits (a full cycle of the test pattern). Word Sync is used to mark each test cycle and is available as an auxiliary output, TRANSMITTED WORD SYNC.

4.3.9 Zero Suppression/Logical Error Insertion

Zero suppression is a process which limits the number of consecutive zeros produced by the Sequence Generator to conform with accepted Bell System standards. Consecutive zero patterns are limited to fourteen when operated at the T1 Bit Rate. When operating at the T1C Bit Rate, no zero suppression is required resulting in patterns up to nineteen zeros long (maximum permissible sequence generator pattern). A strap option located on the APS/BUFFER module (A7) will assert fourteen zero suppression at both the T1 and T1C rates.

Zero suppression is attained by inverting the data pattern exiting the twentieth stage of the Sequence Generator. The first zeros in excess of fourteen are inverted (0 to 1). This is accomplished by the Zero Counter which identifies zero patterns greater than fourteen two clock periods before the first zero will exit the Generator. Flip-flops U19A, B and U21A form a three bit shift register. Zero suppression information is inserted into the second stage (U19B) through U20A. This signalling is inhibited by U22D when operating at T1C. Flip-flop U19A and other logic operated during logical error insertion. The suppression information arrives at the Invert Gate within two clock pulses synchronously with emergance of the first zero from the Sequence Generator.

Operation of the zero suppression circuits is modified slightly when logical errors are inserted. As discussed in Section 4.1.1, logical errors are inserted by inverting the bit just prior to zero suppression and another just after, for each occurence of seventeen or more zeros. This is accomplished by setting the first and last stages (U19A, U21A) of the zero suppression shift register at the same time the second stage (U19B) is set by zero suppression information. Within one clock pulse the Invert Gate will be signalled to invert the output of the Sequence Generator which is just one bit before the occurrence of the Detected Zero Pattern. When the end of the zero pattern is detected by the Zero Counter all inputs to the zero suppression circuit are removed. The next two clock pulses invert the pattern as required for zero suppression. The third clock pulse inverts the first zero of the suppressed fourteen zero pattern producing an error. Patterns of seventeen or more zeros occur four times each generator cycle. Two errors are inserted each pattern for a total of eight errors each cycle of 1,048,575 bits.

4.3.10 Invert Gate

An exclusive-OR gate (U9B) inverts the output of the Sequence Generator when signalled by the zero suppression logic.

4.3.11 Data Selector

A Data Selector composed of U6 directs either the output of the Invert Gate or Received data to the Bipolar converter. When the MODE switch is operated to APS, the Receive data is selected.

4.3.12 Bipolar Converter

The output of the Data Selector is sampled and delayed one-half bit by the sampling flip-flop (U10). The output of the flip-flop is then ANDed with Clock pulses through U22A to obtain a return to zero (RZ) data format for the Bipolar Converter.

A single flip-flop and two gates (U5C, U5D) make up the Bipolar Converter. Its function is to alternate the polarity of all 1's in the test sequence, regardless of the interspersion of 0's; thus, when a 1 is generated of one polarity, the next 1 will have the opposite polarity, whether or not there are 0's between the two 1's.

Bipolarization is triggered by the trailing edge of each 1 in the data stream. At this instant, the flip-flop toggles so that the next 1 is transmitted with the opposite polarity. Two gates, U5C and D, delay the toggle input to the flip-flop slightly to ensure a correct time relationship with the inhibit input from the Bipolar Violations Control Circuit. Outputs from the flip-flop are passed to the line driver to control the polarity of the transmitted signal.

4.3.13 Line Driver

Each of the Bipolar Converters two outputs are directed to a Line Driver U23. The Line Driver contains two AND gates with associated drive transistors. These internal transistors conduct alternately under the direction of the Bipolar Converter and data to be transmitted. Each transistor drives one primary winding of T1.

The transformer is trifilar wound, with two of its winding connected at the center-tapped primary. The third winding serves as the balanced output, which is padded as necessary and distributed to the DS1/DS1C OUTPUT jacks and to the Receiver. Shaping the inherently rectangular signal bits into the T1 pulse shape with trailing edge overshoot is accomplished with a passive RLC circuit (R9, R10, L1, C1) connected across the transformer primary. This wave shaping circuit is connected for T1 (DS1) data rates only. At the T1C rate FET Q1 represents a high source to drain resistance. FET Q1 is controlled by a level shifting circuit Q2 and Q3. The Bit Rate switch (T1/T1C) turns Q2 and Q3 on when operated to T1C. This applies -5 volts to the gate of Q1 turning it off.

The Gas Spark Gap GS1 protects the line driver from large line transient voltages.

Resistors R18 through R27 serve to drop the output voltage to 3 volts peak while providing a measure of isolation between outputs and a 100 ohm output impedance. These resistors link the line driver to the four DS1/DS1C outputs and provides a loopback path from the Transmitter to the Receiver for Self Test purposes.

4.3.14 Violations Control

Insertion. Flip-flops U14 and 21B form a three stage flip-flop which is clocked by data from the Sequence Generator. Violations are inserted by inhibiting the flip-flop U12 in the Bipolar converter circuit following the format decribed in Section 4.1.1. The Violations Circuit is signaled with a Zero Decoder output which has been synchronized to the transmitted data by the External Error Interface Circuit.

4.3.15 External Error Interface

Signals and synchronizes them to the Transmitter Clock and Transmitter Data.

Logical error synchronization to the Transmitter Clock is acheived by U17A and B. A positive transition of the external errors control sets the output of U17A. The next positive transition of the Transmitter Clock sets U17B and resets U17A. The output of U17B has a duration of one clock cycle and signals the logical error circuit to insert one error.

Violations synchronization to the transmitter data is achieved by U15A and B. Operation is identical to the logical errors circuit with the transmitter data used in place of the Clock.

4.4 RECEIVER CIRCUITS

4.4.1 Loopback Control

Loopback between Transmitter and Receiver is controlled by a reed relay (K3). The loop is normally closed, and is opened by insertion of a plug into the DS1/DS1C INPUT jack or by holding the SELF TEST switch at its INTERRUPT DATA position. The relay is de-energized when the loop is open.

4.4.2 Receiver Module (A3)

4.4.2.1 Variable Threshold

The main purpose of the Variable Threshold Front End is to provide a high impedance (1K ohm at T1C) input to the incoming signal, and provide output signals to the slicer circuit (4.4.2.2) from which it can extract the positive and negative bipolar signals.

The input signal is transformer coupled (T2) to the gate of the input stage Q14. The transformer and FET combine to provide a high impedance. The output of the FET follower is capacitively coupled to the base of Q2, the gain of which is adjusted to 6 dB via select resistor R9 (nominally 2K ohm). This stage compensates for the loss through transformer T2.

Emitter follower Q1 is used to drive transformer T1 which splits the incoming bipolar waveform into two waveforms 180° out of phase. One waveform consists of positive pulses for positive voltage 1's and the other consists of negative pulses for negative voltage 1's. These two signals are then fed to the slicer circuitry.

4.4.2.2 Slicer

The Slicer combines two separate functions. First it sets an amplitude threshold which recognizes a "1" or "0" logic data level. Second, it separates the positive and negative bipolar levels into two separate data signals which are T^2L compatible.

Integrated Circuit (U1) consists of five matched transistors, two of which (Q3, Q4 with C8 and R3) form a peak detector which is used as a reference for detection of a logic "1". Transistors Q1 and Q2 present high impedance loads to the transformer outputs and low impedance outputs to comparator (U2). The fifth transistor Q5 is connected as a diode and is used to compensate for the Vbe loss across the other transistors. U2 consists of two comparator circuits, the negative input of each is tied together and to the peak detector's output. The positive inputs are fed from the two output pulse streams from U1 (Q1, Q2). The two outputs of this chip are now unipolar T^2L compatible levels one of which is from positive 1's and the other is from negative 1's. These lines (bipolar A and bipolar B) are used for clock extraction, and all waveform analysis done on the Receiver reference card.

4.4.2.3 Automatic Line Build Out (ALBO)

phase characteristics force its output signal (TP1) to look as if it were at the end of 4000 ft. of cable independent of the cable length terminated by the DS1/DS1C input. The amount of attenuation introduced is controlled by a DC level (TP5) from the AGC circuits.

The received bipolar data is transformer coupled (2:1 ratio) to a high ohms at the T1C rate is attained.

The output of the FET follower is capacitively coupled to the base of Q13, an emitter follower. Resistors R36, 38, 39 determine the quiescent operating point of this and subsequent stages.

Emitter follower Q13 drives the first of two attenuator sections. The first section consists of R33, R34, C13, L5. A DC blocking capacitor C12 connects Q19 and R62. Field effect transistor Q19 is operated in the resistive mode and is dependant on the control voltage from the AGC circuit. The combination of R62 and Q19 adjust the Loss/Phase characteristics of the section.

A Darlington connected transistor pair Q11 and Q12 provide an interface between the first and second attenuator sections. The second section is composed of R43 and L4. Capacitor C11 provides AC coupling to the dynamic resistance created by R57 and FET Q18. The FET operates in the resistive mode and is controlled by the AGC circuit. Emitter follower Q10 interfaces the ALBO with the equalizer.

4.4.2.4 Equalizer

The intent of the Equalizer is to remove the amplitude and phase distortion which would develop from transmitting a 3V bipolar signal down 4000 ft. of cable. Two filter sections and a gain stage accomplish this task.

4.4.2.5 Automatic Gain Control (ACG)

output at approximately two volts peak. Major circuit components are peak detector (Q15) and differential amplifier (Q16, Q17).

Transistor Q15 conducts each time the output of the Equalizer exceeds the voltage across C20 plus one diode drop. Therefore, the voltage across C20 represents the peak output of the equalizer. Resistor R50 and C22 provide ripple filtration.

R52, selected during calibration.

4.4.3 Receiver Reference (A10)

4.4.3.1 Sampling Flip-Flops

Positive and negative data bits from the outputs of the slicer (receiver module) are channelled to the input of two D-type flip-flops (U4A and B respectively). Sampling is achieved by clocking these flip-flops with the receive data clock.

4.4.3.2 Bipolar/Unipolar Converter

Conversion to a unipolar NRZ (nonreturn-to zero) format is accomplished by ORing together the outputs of sampling flip-flops U4A and B. The OR function is provided by U3A.

4.4.3.3 Bipolar Violations Detector

This circuit consists of two-2-stage binary counters (U5 and U6), a gate for each counter ANDs the Receiver Clock pulses with a Slicer output to give Return to Zero (RZ) signals which toggle and reset the counters.

When a 1 of positive polarity is received, the first stage of one counter is set and the second counter is cleared. If the next "1" received is also of positive polarity, another count will be added to the first counter, indicating the occurrence of a violation; however, if the next "1" had been of negative polarity, this counter would have cleared and a count of one would have registered in the first stage of the second counter.

ORing the two counter outputs and ANDing the result with the unipolar data stream completes the bipolar violations detection process. The resultant violations data is channelled to the Error Counter for subsequent display, provided the MODE switch is set for VIOLATIONS.

4.4.3.4 Clock Extractors

internal clock, so that it can properly synchronize with incoming signals.

multivibrator U12A. Constant width pulses produced by the multivibrator add energy to the tank circuits driven by transistors Q1 and Q2. Tank circuits C6, L1 and C9, L2 are tuned to 1.544 MHz (T1 and 3.152 MHz (T1C) respectively. Pulsing these HIGH-Q circuits causes them to ring at their respective frequencies. Each tank circuit drives a two transistor Darlington emitter follower (Q5, 3 and Q6, 4) followed by a phase shift circuit and slicer (U14). Finally, one of the two clocks is selected by the BIT RATE Switch (T1/T1C) working in conjunction with U15A.

4.4.3.5 NO DATA/LOST DATA Detector

These two circuits provide coverage of data loss from the instant of
provides visual warning via the NO DATA indicator when data is not being presented to the Receiver. The Lost Data Detector shows loss of data via the LOST DATA indicator, which goes on with the return of data and remains on until the RESET/RESYNC switch is activated.

The No Data Detector, consisting of U8 monitors the output of the slicers through U2B. The dual retriggerable monostable multivibrator IC8 is connected in a tandem arrangement, where the second state is triggered by an output of the first. The first stage is continuously retriggered by data pulses from the output of IC2B. In the event that data is interrupted, retriggering is discontinued, permitting this stage to complete its monostable function. The time constant of the first stage (26.5 microseconds) is determined by circuit elements R3 and C2. This time constant corresponds to 41 ± 9 T1 time slots. An output from this stage is applied to the gate input of the first stage which inhibits triggering of the first stage for a 100 ms period following detection of No Data. The 100 ms time constant is determined by components R4 and C3. The output of the No Data circuit is extracted from the first stage. This output is directed to both the No Data indicator buffer through U1F and to the clock extractor circuit U2A. Flip-flop U16 controls the LOST DATA indicator. It is set whenever the NO DATA indicator goes off and is reset only by actuation of the RESET/RESYNC switch.

3.4.3.6 ALL 1's

The all 1's circuit identifies received data patterns which contain more than 1024 consecutive 1's and lights the Receiver Status ALL 1's indicator.

Three serially connected binary counters (U10, 11, 17) are permitted to count clock pulses whenever the unipolar data registers a "1". These counters are reset to zero for each occurance of a "0". If the data contains one hundreds consecutive 1's, U17 overflows and sets flip-flop U9B. An output of U9B turns on the ALL 1's indicator through U13B. When a "0" in the data is detected U10, 11, 17 and 9B are immediately reset.

Flip-flop U9B triggers monostable multivibrator U12B which continues to hold the ALL 1's indicator on for another 100 ms. This delay provides sufficient time for the eye to detect the presence of all 1's patterns of only one hundred bit times (65 microsec, T1).

4.4.3.7 Strap Option A

This option allows the binary counters to accept up to one thousand and twenty-four (1024) consecutive 1's.

4.4.4 Receiver Logic (A5 Module)

4.4.4.1 Receiver Sequence Generator

The Receiver Sequence Generator produces a test sequence identical to that of its Transmitter counterpart. Its outputs are taken from different stages of the shift register, its timing is derived by extracting clock pulses from incoming data, and its feedback loop may be opened to receive incoming data for the purpose of synchronization with this data. Generator components are U1, 2, 3, 5; 10A serves as the exclusive-OR circuit in the feedback link. The bridge between stages 17 and 18 contains the Loop Control circuitry which opens or closes the feedback loop (U4).

With the feedback loop closed, the Receiver Generator behaves exactly as the Transmitter Generator in working up the 1,048,575 bit test sequence, but it is necessary to synchronize the test sequence from the Receiver Generator with that of an incoming signal if a bit-by-bit comparison of data bits is to be performed. This synchronization is achieved by opening the feedback loop and inserting the incoming signal in place of the Generator's output. The Generator responds as if the loop were closed, and within a very brief time interval (twenty data bits later), the Generator's output corresponds exactly with the data being inserted in its place.

Should incoming data contain error bits during synchronization, the process will be delayed. In order for synchronization to be achieved, incoming data must contain at least twenty error-free bits; an additional forty error-free bits must be received in order to confirm synchronization. Once synchronization is confirmed, the Generator's Sync Control circuit forces the feedback loop to its closed status so that normal operation may resume.

Should synchronization be lost during normal operation, the loss is detected by the Out-of Sync Detector. In the AUTO mode, this circuit then signals the Sync Control to reopen the feedback loop for resynchronization. Resynchronization in the MANUAL mode is initiated by actuating the RESET/RESYNC switch.

4.4.4.2 Loop Control

A gate system (U4A,B,C) effectively forms an SPDT switch which controls the Receiver Generator's feedback loop. The input to stage 18 from U4C is the common line. When the loop is closed, stage 18 receives data directly from the output of state 17; when the loop is open, it receives the incoming unipolar data signal. Should synchronization be required, the Sync Control may force the Loop Control to switch stage 18 to the incoming data line. If the Generator is properly synchronized to incoming data, there will be no signal from the Sync Control, and the Loop Control will, therefore, switch data from stage 17 to stage 18.

4.4.4.3 Receiver Zero Counters

Two zero counters are required to effectively control the Sequence Generator. One zero counter (U6, U9A) detects the presence of fourteen or more zeros at the third stage of the sequence generator. When operating at the T1 data rate, an output of flip-flop U9A signals the Invert Data circuit, limiting the number of consecutive zeros exiting the Sequence Generator to fourteen without disturbing the contents of the shift register.

A second zero counter (U32, 33) monitors the nineteenth stage of the Sequence Generator. This generator detects pattern lengths of nineteen and twenty zeros. The nineteen zero pattern defines the RECEIVER WORD SYNC pulse. Twenty or more zeros stimulates the Self Start Circuit.

4.4.4.4 Self-Start

Operation and function of this circuit (U8A) are identical to the Transmitter equivalent. Its input is taken from the Second Zero Counter and its output is routed to the Sequence Generator's 19th stage.

4.4.4.5 Zero Suppression Control

The Receiver Zero Suppression Control circuit operates in a manner similar to its Transmitter counterpart. The Sequence Generator is capable of producing a sequence of up to twenty 0's. To meet the required pattern specifications, it is necessary to limit 0 sequences to a maximum of fourteen by converting any additional 0's to 1's, when operating at the T1 Bit Rate. The control signal from U9A informs the Invert Data Gate (U10B) as to which of the output data bits are to be converted from 0's to 1's.

4.4.4.6 Comparison Gate

The Comparison Gate (U10C) is an exclusive-OR used to compare the received data stream from the Bipolar/Unipolar Converter with the test pattern from the Sequence Generator. Comparison is performed bit-by-bit, and any differences appear as logical 1's at the output of the Comparison Gate.

4.4.4.7 Violations/Errors Sampling

This circuitry samples detected violations and logical errors with the Receiver Clock to eliminate pulse transients which occur in the comparison logic. The MODE switch interacts with sampling flip-flops U11A and B to select either a logic or violations error mode. The outputs of these flip-flops are directed to NAND gate U12B through U12A. U12B combines the error signal and Receiver Clock to produce individual error pulses one-half bit time long. These errors are subsequently directed to the Error Counter.

4.4.4.8 Out of Sync Detector

The Out of Sync Detector monitors outputs from the Violations/Errors Sampling circuit, Error Counter and Bit Counter (Par. 4.4.3.8 and 4.4.3.9). When an out of sync condition is detected, a control signal is sent to the Loop Control which injects received data into the Sequence Generator. After a period of forty error free bits, synchronization is considered re-established and the loop is directed to close.

A two stage shift register (U16A and B) is clocked by an output of the Bit Counter which occurs every twenty bits. If the RESET/RESYNC switch is actuated, U16A and B are set by a short pulse generated by differentiator C6 and R10.

A set condition on U16B steers error pulses to the preset inputs of the shift register via U17A. After a period of twenty bit times, U16A becomes cleared when clocked by the Bit Counter. After another period of twenty bits, U16B is cleared when clocked provided an error has not occurred during the last twenty bits. A detection on one error during this time sets both shift register stages, starting the process over. An output from U16B illuminates the NO SYNC indicator through U13D. When Sync is restored, U15B is clocked, setting this flip-flop and illuminating the LOST SYNC indicator through U13C. Both indicators are held on by alternate inputs of U13C and D when the MODE switch is either in the VIOLATIONS or APS position. Flip-flop U15 is reset by actuating the RESET/RESYNC switch.

Loss of synchronization is determined by an interaction between the Error Counter and Bit Counter. The Error Counter counts detected errors and is reset by the Bit Counter, which counts clock cycles (Bit Slots). Both counters are operator programmable by strapping terminal pairs B1, A1, B2, A2. With no straps, the Error Counter will be reset after the passage of fourty bits. Straps A2 and B2 provide reset after 400 and 4000 bits. Similarly, the Error Counter will overflow after the passage of twelve errors with no straps. Setting straps A1 and B1 provide error counts of 120 and 1200. The unit is shipped from the factory with no straps. Therefore, after the passage of 40 bits, the Error Counter will be reset. However, if more than twelve errors occur within 40 bits, the Error Counter will overflow signalling an out of sync condition having a threshold of twelve errors in fourty bits. The strap options provide thresholds of: 12 in 400 or 4000, 120 in 400 or 4000 and 1200 in 4000.

When overflow occurs, the Error Counter signals U18A which sets the shift register (U16A and B). If the SYNC MODE switch is set to the AUTO position, the Loop Control will again insert received data into the Sequence Generator and the process described for the RESET/RESYNC switch earlier will commence. However, if the MANUAL position is chosen, an auxilliary input to U17D will prevent the Loop Control from inserting received data and a NO SYNC condition will prevail until operation of the RESET/RESYNC switch.

4.4.4.9 Error Counter

The Error Counter consists of three decade counters (U21, 22, 23), a flip-flop (U19) and decoded gates. Errors from the Violations/ Errors sampling circuit are counted with reset provided by a pulse from the Bit Counter. Decoding logic determine error counts at 12, 120, 1200 levels. U27A combines outputs of U21 and 22 to produce a pulse every 12 errors. Gates U27B and U28A decode 120 and 1200 counts respectively. These decoded outputs are combined by U27C and inverted by U28B which provides an overflow signal to the OUT OF SYNC Detector.

With out straps, decoder U27A (Decode 12) occurs prior to outputs of U27B and U28A. This is, therefore, the dominant decoder. If strap A1 is asserted, U27A is inhibited and U27B (Decode 120) becomes dominant. Further, if straps A1 and B1 are asserted, decoder 28A becomes dominent (Decode 1200).

4.4.4.10 Bit Counter

The Bit Counter is essentially a programmable decade counter which outputs a clock to the OUT OF SYNC Detector every twenty bits and a reset signal to the Error Counter every 40, 400 or 4000 bits as programmed by straps A2 and B2.

Decade Counter U24 and flip-flop U20A divide the Receiver Clock by twenty. This provides Clock for the OUT OF SYNC Detector. Outputs from flip-flop U20B, decade counters U25 and U26 continue the divider chain to 40, 400 and 4000 bits. Steering logic, U30A, B, C and U31A, B work in conjunction with straps A2 and B2 to select one of these three outputs. No straps select the 40 bit output. Strap A2 selects 400 and strap A2 plus B2 selects 4000 bits. Flip-flops U29A and B with gates U28B and C generate a reset signal at the end of the selected bit interval which resets U25, U26, U20B and the Error Counter. A preset input to flip-flop U29A, asserted when the Error Counter overflows, forces an early reset signal coincident with the detection of an out of sync condition. This process helps to reduce the number of bit times required to recognize and re-establish synchronization.

4.4.5 Display Logic Module (A8)

4.4.5.1 Error Format

The Error Format circuit accepts detected individual errors (Logical or Violations) and converts them to errored sec., error sec. and 0.3 ms blank formats as selected by the DISPLAY FORMAT switch. The errored sec. mode establishes consecutive blocks of data one second long. One or more errors detected in a block is converted to a single error pulse which will be subsequently counted by the Display Error Counter. The error count is asynchronized to the free running one second period of the timer counter. Error Sec. is

identical to Errored Sec except error count is triggered by the detection of an error. One or more errors detected in the second are counted as a single error. At the end of a second, the count circuit assumes a quiescent state until the detection of another error and the one second count cycle is resumed. This count is termed synchronous as the count is synchronized with the appearance of data errors. In the 0.3 MS BLANK mode, the circuitry waits for the detection of an Error and then inhibits (blanks) the Display Error Counter from counting errors for a period of 0.3 ms after this first error is registered. The Individual mode permits counting of all errors as they are detected.

Detected errors are directed to one input of NAND gate U13A. This gate permits errors to pass only during a count interval. The output is inverted and applied to the clock input of U15A. When the individual mode is selected, the "D" input to this flip-flop is held low resulting in a Hi output from U15A irrespective of the number of errors presented to the clock input. U12C functions to combine the output of U15A and U13A. With the output of U15A high, all errors gaged by U13A are passed to the Display Counter.

With the DISPLAY FORMAT switch set to ERRORED SEC., errors at the clock input of flip-flop U15A set the output low. This action prohibits U12C from passing individual errors to the display Counter and removes the reset applied to oscillator U14. The oscillator produces a clock rate of ten cycles per sec. which is divided by ten with decade counter U16. Steering logic U17 directs the output of counter U16 to the differentiator U18A, B, C and C18. This circuit produces a narrow negative transition pulse for each negative transition of U17A. The output of flip-flop U15A is thus cleared after a period of one second producing one error pulse for one or more errors in a one second block. Under error free conditions, U15A is simply reset every second. But, since it was not set by an error, no error pulse is generated.

Operation in the Error Sec mode is similar to the Errored Sec mode except it is synchronous to the error occured. When the switch is in the Error Sec mode, the output of U13D is low. This condition inhibits oscillator U14. Once an error occurs, it passes the first error to the error count through U12C, and then changes the output of U15A to low. This action prohibits counting any more errors as well as enables the oscillator to start counting one second timing. When one second is up, the output of U18A will send out a pulse to set the output U15A to the high state. This action will allow the new cycle to start whenever error reoccurs.

When switched to the 0.3 ms Blank mode, the oscillator U14 is adjusted to generate a clock of 0.3 ms period. Resistors R34, R35, R36 and capacitor C14 determines the 0.3 ms rate. The switch is made by turning on Transistor Q1 which places R33, 32 in parallel with R34, R35, reducing the circuits time constant. Reset of flip-flop U15A is now determined by the 0.3 ms rate. However, reset does not occur continuously. One input of U13D is held high by the DISPLAY FORMAT switch and inverter U13C. When U15A is reset, oscillator U14 is also held in reset. An error sets U15A and removes the reset on U14 allowing it to complete a 0.3 ms cycle. This, in turn, resets U15A after 0.3 ms. Errors occurring during this period are blocked by U12 and associated output of U15A. The result is one error pulse for one or more errors during the 0.3 ms period.

4.4.5.2 Display Multiplexer Control

The Display is multiplexed by digit (most significant, MSD, to least significant, LSD), and by function (error count or timer status).

The digit mux. rate is determined by oscillator U1 in conjunction with R1, 2 and C2 which set the time constant. Inverter U5A connects the oscillator with Johnson Counter U2A, B. Outputs of the counter are decoded by U3A, B, C, D. These outputs are connected to the DISPLAY Module to scan the three digits sequentially and reset the leading zero suppression control.

When the Test Set is operated in the APS mode, the Counter U2 is held reset by U32. This effectively blanks the three digit display.

A common BCD data bus (wire OR-ed) connects the three digits of the Error Display Counter and Timer Counter with the Display Module. Selection of the Timer Counter (TIMER STATUS) is determined by gate logic U5B, C, D. Similar circuits on the BUFFER/APS module select the Error Display Counter. The TIMER STATUS switch determines which function is to be displayed.

4.4.5.3 Timer Counter

The Timer consists of three presettable decade counters U6, 8, 10. These counters are preset by BCD data (complement, BCD) from the TIMER thumbwheel switches when the RESET/RESYNC switch is operated. A clock having a period of one minute forces the counters to count down from their preset value to zero. The zero condition signals the Count Control to end the Count Interval. The status of the Timer (test time remaining) can be displayed by operating the TIMER STATUS switch. Open collector gates U7, U9, U11 in conjunction with signals from the Display Mux. control place the Timer Counter outputs on the Data Bus (MSD to LSD).

4.4.5.4 Bit/Time Interval Control

The Bit/Time Interval Control determines the test length (count interval) in either bits (10^6, 10^7, 10^8, 10^9) continuous, or TIMER (1 to 999 minutes) as selected by the COUNT INTERVAL (Bits) switch. Bit rates are determined by the Receiver Word Sync signal which is generated every 1,048,575 bits (10^6).

Three decade counters U23, 24, 25 and selection logic U20A, B, C, U21B determine the bit rates: 10^6, 10^7, 10^8, 10^9.

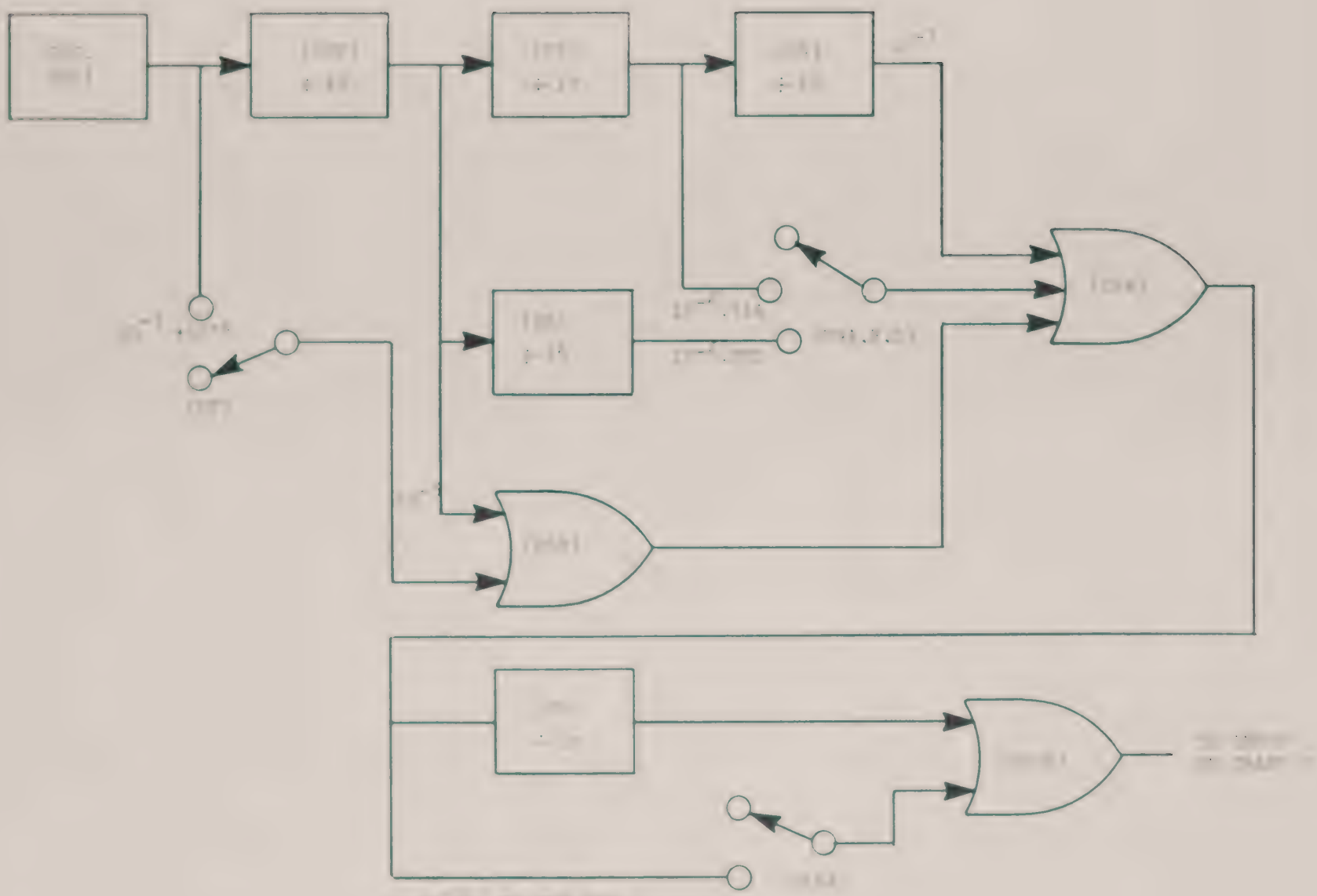
The one minute clock pulses required by the Timer Counter are derived from the Word Sync signal by forcing counters U23, 24, 25 to divide by 88 for T1 and 180 for T1C bit rates. U26A decodes 88 if the BIT RATE switch is set to T1 while U26B decodes 180. Flip-flop U28 produces a pulse, one Receiver Clcok period in width, every 88 or 180 Word Sync cycles. If a count interval is in process, U27C directs one minute clock pulses to the Timer Counter through inverter U27D and resets U23, 24, 25 through U27B.

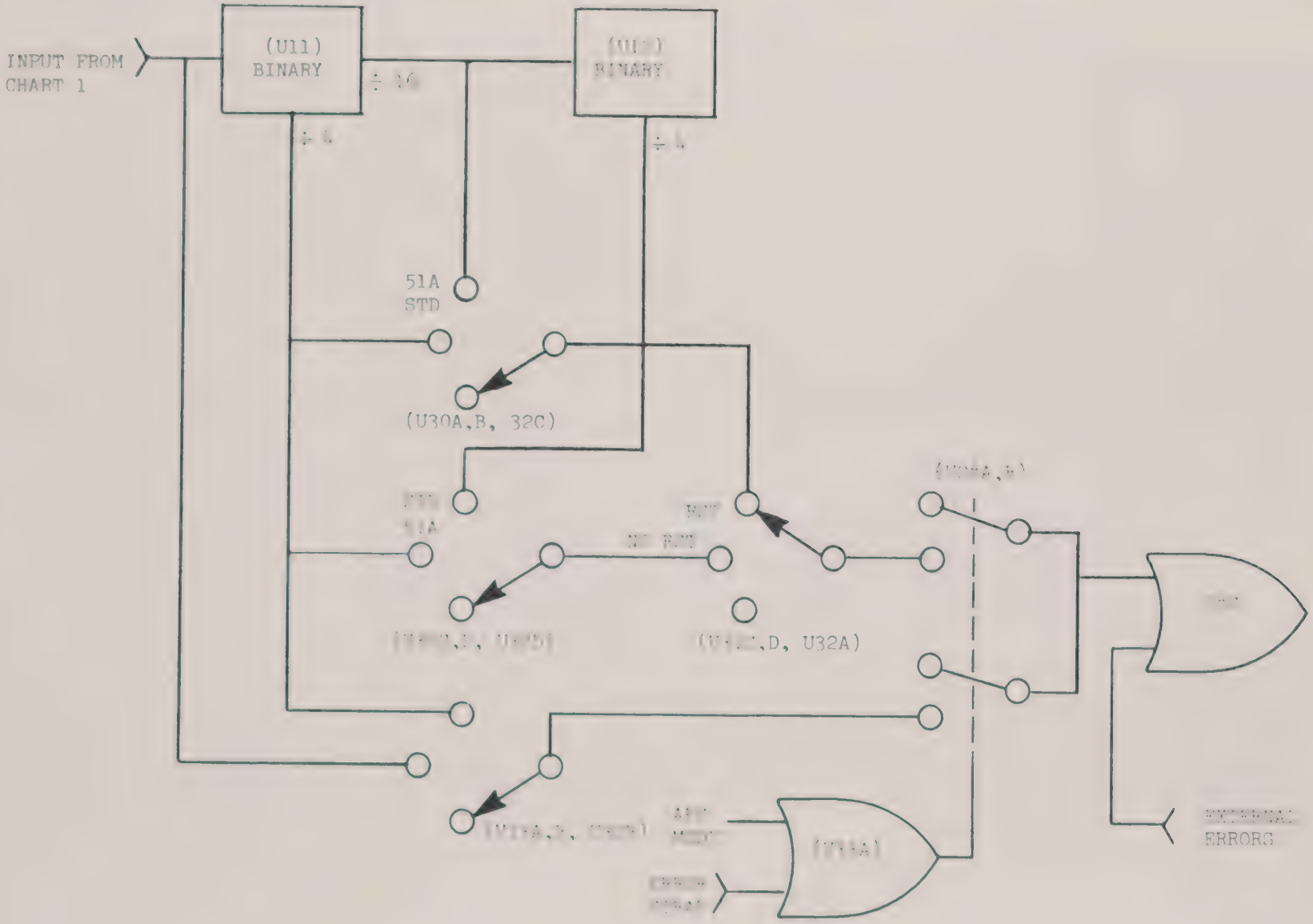
Gates U20A, B, C, D, U21B, C, U19A, B, C direct appropriately selected bit rate or timer, count interval completed, signals to the Count Control circuits.

4.4.5.5 Display Interval

The length of time (1 - 10 sec and hold) that the final results of a completed counter interval are displayed before testing is restarted is determined by this control. A monostable oscillator U30 in conjunction with the DISPLAY INTERVAL CONTROL, R37, 38 and C11 determine display time.

The hold feature is executed by turning transistor Q2 on which restricts capacitor C11 from charging. Completion of a Display Interval signals the Count Control to start another count interval.




INPUT FROM
CHART 1
(U11)
BINARY
÷ 4
51A
STD
(U30A,B, 32C)
(U32C,D, U32A)
ERRORS

4.4.5.6 Count Control

The Count Control issued signals to other circuits which determine the test length (count interval).

Flip-flop U31A is cleared by a signal from the Display interval control when clocked by the Word Sync signal. This action creates a reset signal which resets the Error Display Counter and loads the Timer Counter. The next occurence of the Word Sync signal clears flip-flop U15B and starts the count interval. The negative transition of the Word Sync clears U31B which in turn sets U31A removing the reset signal. U15B is clocked by an output of the BIT/TIME interval control which terminates the count interval, provided the COUNT INTERVAL (Bits) switch is not set to CONT (continuous). This condition holds the D input of flip-flop U15B low, preventing it from setting. An output from U15B is directed to Q2 of the Display Interval circuit to stimulate the beginning of another count interval through U12D. An auxilliary input to U12D inhibits this process when the COUNT INTERVAL (Bits) switch is set to TIMER. This effectively holds the Display regardless of the DISPLAY INTERVAL control's position.

4.4.6 BUFFER/APS MODULE (A7)

4.4.6.1 APS Violations Control

The APS VIOLATIONS CONTROL determines the violation insertion rate when the Test Set is operated in the APS mode. An output from this circuit stimulates violations control circuits on the Transmitter module. RANGE, SEQUENCE and STD/51A front panel switches determine the rate of violation insertion.

Oscillator U1 generates a 3081 Hz square wave which acts as a time base for an elaborate jitter scheme. The circuit time constant is dependent on R5, 6, 7 and C22. At the time of this writing, automatic protection switches were not available for T1C channels. In anticipation for future expantion to T1C, transistor circuit Q1 has been added, which places R2, 4 in parallel with R5, 6 to adjust the circuit time constant.

4.4.6.2 Error Display Counter

The Error display Counter tallies errors presented to it from the Error Format circuit. Counter outputs are multiplexed and placed on a data bus which interconnects the Error Display Counter, Timer Counter and Display.

A three digit BCD counter is formed using decade counters U17, U19, U21. Outputs of these counters are multiplexed by open collector NAND gates U18, U20, U22 in a wire-OR configuration. Multiplex control signals are steered to these gates by U14A, B, C and inverter U15. Transfer of these outputs to the bus is inhibited when the TIMER STATUS switch is operated.

4.4.6.3 Strap Options

Strap option "B" modifies the transmitter and receiver Sequence Generators to produce patterns limited to fourteen zeros at both the T1 and T1C bit rates. The Test Set is manufactured without this strap which provides fourteen zero suppression at T1 and no suppression at T1C (up to nineteen consecutive zeros).

Violation error rates generated by the APS circuits are normally available only with the MODE switch in the APS position. This lock out feature prevents accidental error insertion should the SEQUENCE switch be in a position other than START. However, some operators may find these error rates useful for other testing in the VIOLATIONS or LOGIC mode. A strap option has been provided (strap A or Pin 48 on INTERFACE CONNECTOR) which will override this lock out feature.

4.4.6.4 Printer/Remote Interface (Option P)

This interface permits the connection of a printer to the 273 and remote operation of some front panel controls. Connection to the printer is established through three parallel BCD data paths, one path for each digit of the Display Error counter. The BCD is available at twelve pins of the Interface connector in complement BCD format, TTL levels.

Outputs of the Error Display counter U17, U19, U21 are buffered and inverted by U23 and 24. A carry signal (10 ms pulse) is generated by U27 each time the most significant counter (U21) overflows. The print command (100 ms pulse) is generated at the end of each count interval. (Ref. Para. 3.2).

4.4.7 Display Module (A1)

The DISPLAY MODULE contains the three seven segment LED Displays, the Receive status indicators, RESET/RESYNC switch and TIMER STATUS switch.

Digit drivers (Q1, Q2, Q3) interface with display multiplexing signals from the DISPLAY LOGIC module to scan the Display from the most significant

digit (MSD) U5 to least significant digit (LSD) U7. Display decoder U3 converts the BCD input from the data bus to drive the seven segment LED displays. Resistors R7 through R13 determine the peak segment current.

Flip-flop U4 controls the Display's leading zero blanking. The flip-flop is cleared during a time slot between display of the LSD and MSD digits. An output from decoder U3 holds U4 in its cleared state, if the BCD data for the MSD is zero. Flip-flop U4 signals U3 to blank the Display. If the next digit is non-zero, U4 is set and removes the blank signal from U3. When the Test Set is operated in the APS mode flip-flop U4 is held in the clear state. The COUNT and OVERFLOW indicators are driven by transistors Q4 and Q5. Transistor Q5 is controlled by the same multiplexer signal which clears U4. Therefore, in the APS mode the COUNT and OVERFLOW indicators are held off.

Drivers U1 and U2 provide a buffer between Receiver Status indicators DS1 through DS8 and their respective control logic.

4.4.8 Power Supply Assembly (A6)

The Power Supply for the Test Set is composed of transformer T1, capacitor C1 (both chassis mounted), and Power Supply Assembly (A6). The transformer secondary is center-tapped and drives the full wave rectifier, CR1 and CR2. This Rectifier in conjunction with capacitor C1 provides 48 V DC. The Test Set can be powered by either 115 V AC, using transformer T1, or 48 V DC from an external power source (e.i. telephone central office battery: T1P, -48 V; sleeve, + ground). Diode CR3 interfaces the externally applied 48 V DC power with the internal 48 V DC power derived from the 115 V AC input.

A DC-DC converter consisting of transformer T2, Transistors Q1 and Q2, and bridge rectifier CR5, 6, 7, 8 converts the 48 V DC power to plus and minus 12 V DC. Capacitor C6 is the +12 V DC ripple filter and C7 the -12 V DC filter.

Four linear regulators determine the final power requirements of the Test Set, VR1, 2, 3, 4. Each regulator provides: +6.8 at 50 ma (VR1), +5 V at 1.2 ma (VR2), +5 V adjustable at 250 ma (VR3), and -5 V at 100 ma (VR4). The +5 V power supply (VR2) is overvoltage protected by zener diode CR9.

The Lost Power Circuit consists of detector U1 and reset circuitry Q3 and CR10. Detector U1 is established in the Set "1" state when power is first applied or interrupted for more than one second. In the set state, the lost power indicator is turned on. Reset is accomplished with the operation of the RESET/RESYNC switch and level shifter Q3.

5.0 MAINTENANCE

5.1 Test Equipment Requirements

a. Frequency Counter — GR Model 1191 or equivalent

b. Osicllloscope — Tektronix Model 547 or equivalent

c. Oscilloscope Accessories — Tektronix Model 1A1 Plug-In or equivalent, with 2 each X10 Probes and 1 each X1 Probe (calibrate these items to be compatible with the Oscilloscope to be used).

d. Bell System J98710R T-1 Quasi-Random Signal Source or Dataspeed 40, 40A, B, or C Error Rate Test Set.

e. Tapped Termination, 1 each per Figure 5-1.

f. Termination, 3 each, per Figure 5-2.

g. Resistor, 100 ohms, 1% with an alligator clip at each end.

h. Standard Error Rate Test set. This set must first have been qualified for use as an operating standard by (1) successfully passing Self Test requirements of Section 2.2, and (2) be certified as having synchronized to a Bell System J98710R T-1 Quasi Random Signal Source without recording errors (3) be certified to insert and detect both errors and violations exclusive of one another.

i. Storage Oscilloscope — Tektronix Model 549 or equivalent with a 1A1 Plug In.

j. D.C. Power Supply — Power Designs Model TW5005 or equivalent.

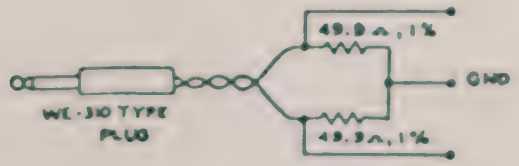


Fig. 5-1: Tapped Termination (1 Required)

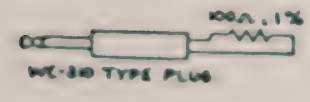


Fig. 5-2: Termination (3 Required)

5.2 Calibration Procedure

5.2.1 Preliminary

(a) Remove the Test Set from its outer case.

CAUTION: Voltages as high as 115 Vac are present in the vicinity of the Power Switch and the Fuseholder.

(b) Apply 115 Vac power to the Test Set and turn on the Power Switch.

(c) Do not connect equipment to the Test Set except as directed below.

5.2.2 Oscillator Frequency Adjustment

(To be made only after a one hour minimum warm-up)

(a) Connect the Frequency Counter to the TRANSMIT BIT SYNC and GRD terminals on the front panel of the Test Set. Set the BIT RATE switch to T1C.

(b) Adjust the counter for a one second count.

(c) Adjust capacitor C14, at the edge of the Transmitter board (A4) for a frequency of 3,152,000 Hz ± 5 Hz.

(d) Set the BIT RATE switch to T1.

(e) Adjust capacitor C18, at the edge of the Transmitter board (A4) for a frequency of 1,544,000 Hz ± 5 Hz.

(f) Disconnect the counter.

5.2.3 Transmitter Amplitude Adjustment

(a) Properly calibrate the Oscilloscope, Plug-In, and X10 Probe with respect to both frequency and amplitude using the internal calibration source.

(b) Plug the test termination shown in Figure 5-1 into one of the four output jacks of the Test Set and set the BIT RATE switch to T1.

(c) Connect an X10 Oscilloscope probe between the GRD terminal and either one of the remaining terminals of the Tapped Termination (Fig. 5-1).

(d) Set the Oscilloscope sweep for 0.1 usec/cm and vertical sensitivity for 0.05V/cm. Adjust potentiometer R6 (+5V Adjust), on the lower edge of the Power Supply board, for a pulse height of 1.5V (3 cm) ± 0.1V peak or 3.0V (6 cm) ± 0.2V peak as shown in Figure 5-3.

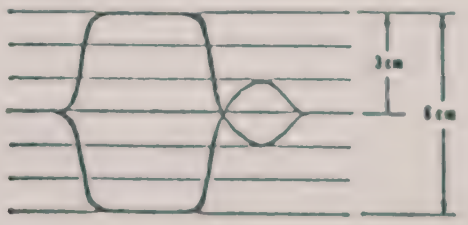


Figure 5-3: Transmitter Amplitude

(e) Disconnect the Oscilloscope Probe and unplug the test termination from the Transmitter output jack.

5.2.4 Receiver AGC (ALBO)

This adjustment is not part of normal maintenance and should be necessary only when repair (component change) is required.

Resistor R49, on the Receiver Module (A3), is a select value determined by Bowmar during factory calibration. This resistor determines the voltage gain of the AGC circuit.

(a) Test Equipment Adjustments

273 Controls:

DISPLAY FORMAT	Individual
BIT INTERVAL	10^{-6}
MODE	Logic
BIT RATE	T1
BRIDGE/TERM	Term

Remove all DS1/DS1C 310 jack inputs and outputs.

Oscilloscope

CH1	X1 Probe, connected to TP7 (ALBO output), amplifier to 50mv/cm.
CH2	X10 Probe, connected to RECEIVER BIT SYNC on front panel, amplifier to 5V/cm.
Time Base	Trigger CH2, 0.5 us/cm.

(b) Temporarily connect R49, a 0.5W 5% 1/4W carbon composition resistor, to terminals provided.

(c) The waveform on CH1 (TP7) should be approximately 100 mv peak (Gain adjustment to follow).

(d) Connect the Oscilloscope's CH1 to TP9 (equalizer output) and adjust CH1 amplitude for 1V/cm. Set the Test Set's BIT RATE switch to T1C.

Observe that there is a slight amplitude imbalance between the positive and negative pulses. Select the pulse of smaller amplitude and adjust R49 for a peak voltage of 0.2V ± .1V measured between the base line and the inner open section of the pulse (Fig. 5-4).

Fig. 5-4

(e) Solder R49 in place. Disconnect all test equipment

5.2.5 Clock Extractor Adjustments

(a) Test Equipment Adjustments

273 Controls	
BIT INTERVAL	10^{-6}
MODE	Logic
BIT RATE	T1
BRIDGE/TERM	Bridge
DISPLAY FORMAT	Single
Oscilloscope	
CH1	X10 Probe to TP2 amplifier to 2V/cm
Time Base	Set to 0.1 us/cm, EXT. SYNC. Connect a X1 Probe between EXT. SYNC. and Xmit BIT SYNC pin jack on front panel

(b) Use a tuning tool to adjust inductor L1 for a symmetrical square wave with clean transitions.

(c) Switch the sweep magnifier to X10 and adjust the Oscilloscope's position controls to bring the positive pulse transition into view (Fig. 5-5).

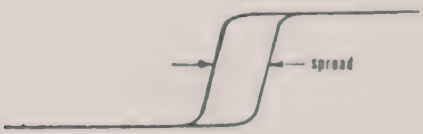


Fig. 5-5

(d) Continue to adjust L1 for a minimum spread on the transition edge, using the Oscilloscope's position controls to keep the pattern centered or conviently located.

(e) Place the 273's BIT RATE switch to T1C and connect the Oscilloscope's CH1 to TP1. Adjust L2 by repeating Steps b, c, and d.

(f) Remove Oscilloscope Probes from test points.

5.2.6 Clock Extractor Phase Adjustment

(a) Test Equipment Adjustments

Oscilloscope

CH1	X10 Probe connected to TP5, amplifier 2V/cm.
CH2	X10 Probe connected to TP3 (U4 Pin 3), amplifier 2V/cm.
Time Base	Adjust for 0.1us/cm and Synce to CH2.

(b) Adjust the Oscilloscope's horizontal position control to set the positive transition of CH1 on the vertical center line (See Fig. 5-6).

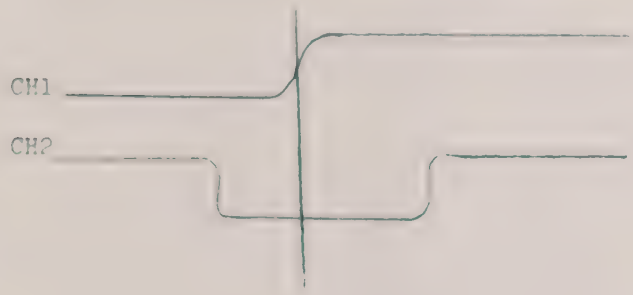


Fig. 5-6

(c) Adjust capacitor C21 to position the CH2 pulse symmetrically around the transition of CH1.

(d) Adjust the 273's BIT RATE switch to T1C.

(e) Adjust C12, following the procedure outlined in Steps b and c.

(f) Disconnect the Oscilloscope.

5.2.7 APS Violations Oscillator

(a) Connect a Frequency counter to TP1 of the Buffer/APS (A7) Board and set the BIT RATE Swtich to T1.

(b) Adjust R5 for a frequency measurement of 3081 Hz ± 5 Hz.

(c) Set the BIT RATE switch to T1C and adjust R6 for a frequency of 6290 ± 10 Hz.

5.2.8 Display Format Oscillator

(a) Connect a frequency counter to TP5 on the DISPLAY LOGIC (A8) board. Set the DISPLAY FORMAT switch to INDIVIDUAL.

(b) Set the counter's controls to make a period measurement (100 ms).

(c) Adjust R35 for a period measurement of 100 ms ± 1 ms.

(d) Connect a temporary jumper between ground (edge of card) and TP6.

(e) Adjust R33 for a period of 0.300 ms ± .001 ms.

5.2.9 Final

(a) Return the test set to its case and secure with the four front panel screws.

(b) Perform the Self Test (Section 2) as a final check of the instrument.

5.3 Performance Checks

5.3.1 Preliminary

These checks are to be made with the Test Set in its case. They may serve for periodic maintenance, quality control checks, and for post-repair checkout. The Error Rate Test Set must be connected to a power source of 115 VAC ± 10%, 50 to 60 Hz.

5.3.2 Transmitter Checks

5.3.2.1 Transmitter Clock Frequency

(a) Allow the Test Set to temperature stabilize by operating for at least one hour at room temperature. The Test Set may be momentarily unplugged only for the purpose of moving it.

(b) Connect the Counter input to the TRANSMITTER BIT SYNC jack and the GRD terminal located in the lower left section of the front panel. Set the BIT RATE switch to T1.

(c) Adjust the Counter for a one-second count interval (to read directly in Hz), and set the Counter's input control for a consistent display. The Counter should register between 1,543,950 and 1,544,050 at the end of each count interval.

(d) Set the BIT RATE switch to T1C. The Counter should register between 3,151,950 and 3,152,050 at the end of each count interval.

(e) Disconnect the Counter.

5.3.2.2 Bipolar Output (T1)

(a) Check calibration of the Oscilloscope and a X10 Probe with respect to frequency compensation and gain, using the internal calibration source of the Oscilloscope and the Oscilloscope manufacturer's procedure.

(b) Connect the cord of the test circuit shown in Figure 5-1 to one of the DS1 Output jacks of the Test Set, and insert the three Terminations (Fig. 5-2) into the remaining output jacks. Attach the GRD lead of the X10 Probe to the GRD, center tap of the test circuit and the Probe tip to either of the outer taps.

(c) Adjust the Oscilloscope for a vertical sensitivity of 0.05V/division and a sweep-rate of 0.1 usec/division (magnifier off). Adjust the trigger, intensity, and position controls to obtain the waveform shown in Figure 5-7.

(d) The measurements designated (1) and (2) in Figure 5-7 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Measurements (1) and (2) should differ by not more than 0.15 cm (0.075 volts).

(e) Measurements (1) and (4) should be between 6.0 and 7.0 cm (300 and 350 nsec). Measurements (3) and (4) should differ by not more than 0.15 cm (15 nsec).

(f) Measurements (3) and (5), taken between 10% and 90% of peak points, should be less than 0.8 cm (80 nsec).

(g) Measurement (6) should be between 10% and 90% of the base line to peak reading (norminally 0.3 to 0.9 cm for a 3.0 cm peak).

(h) Measurement (8), taken 4.0 cm to the right of the point of measurement (7), should be less than 10% of measurement (7) (Note: It may be necessary to increase the vertical sensitivity in order to make this measurement).

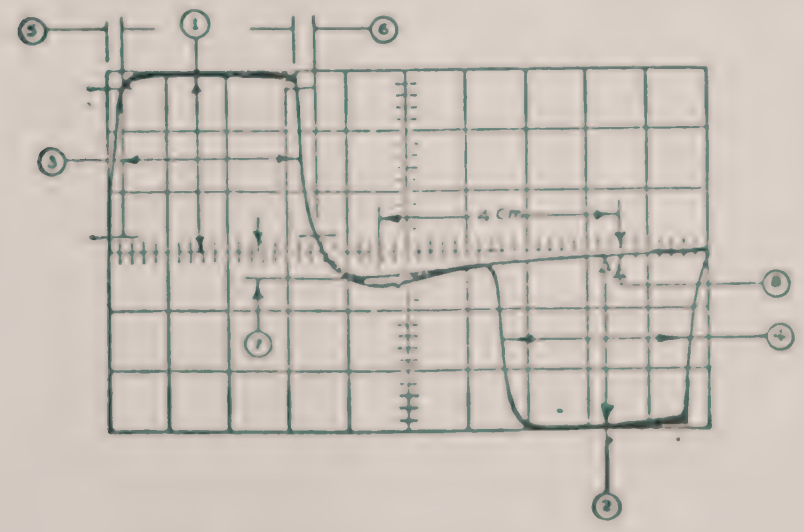


Fig. 5-7: Bipolar Waveform

(i) Exchange output jack connections with the Tapped Termination and one of the three other Terminations. Repeat Steps d through h, above.

(j) Repeat Step i, using a new output jack for the Tapped Termination.

(k) Repeat Step j. The Tapped Termination should now have been used in all four output jacks.

(l) Remove the three terminations one at a time observing the Oscilloscope trace. The trace should not be altered as the terminations are removed. Finally, move the Tapped Termination to one of the three other output jacks. The waveform of Figure 5-7 should reappear on on the Oscilloscope.

5.3.2.3 Bipolar Output (T1C)

(a) Set the BIT RATE switch to T1C, and insert the tapped termination into one of the DS1/DS1C outputs.

(b) Adjust the Oscilloscope for 0.5V/cm and .05us/cm.

(c) The measurements designated (1) and (2) in Fig. 5-7 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Measurement (1) and (2) should differ by not more than 0.15 cm (0.775 volts).

(d) Measurements (3) and (4) should be between 3.9 cm and 4.5 (195 and 175 nsec). These measurements should not differ by more than .3 cm (15 nsec).

(e) Measurements (5) and (6) taken between 10% and 90% of peak points, should be less than .8 cm (40 nsec).

(f) Measurement (7) should not exceed 10% of the peak amplitude .5 cm. CAUTION: Poor Probe grounding will greatly affect this measurement.

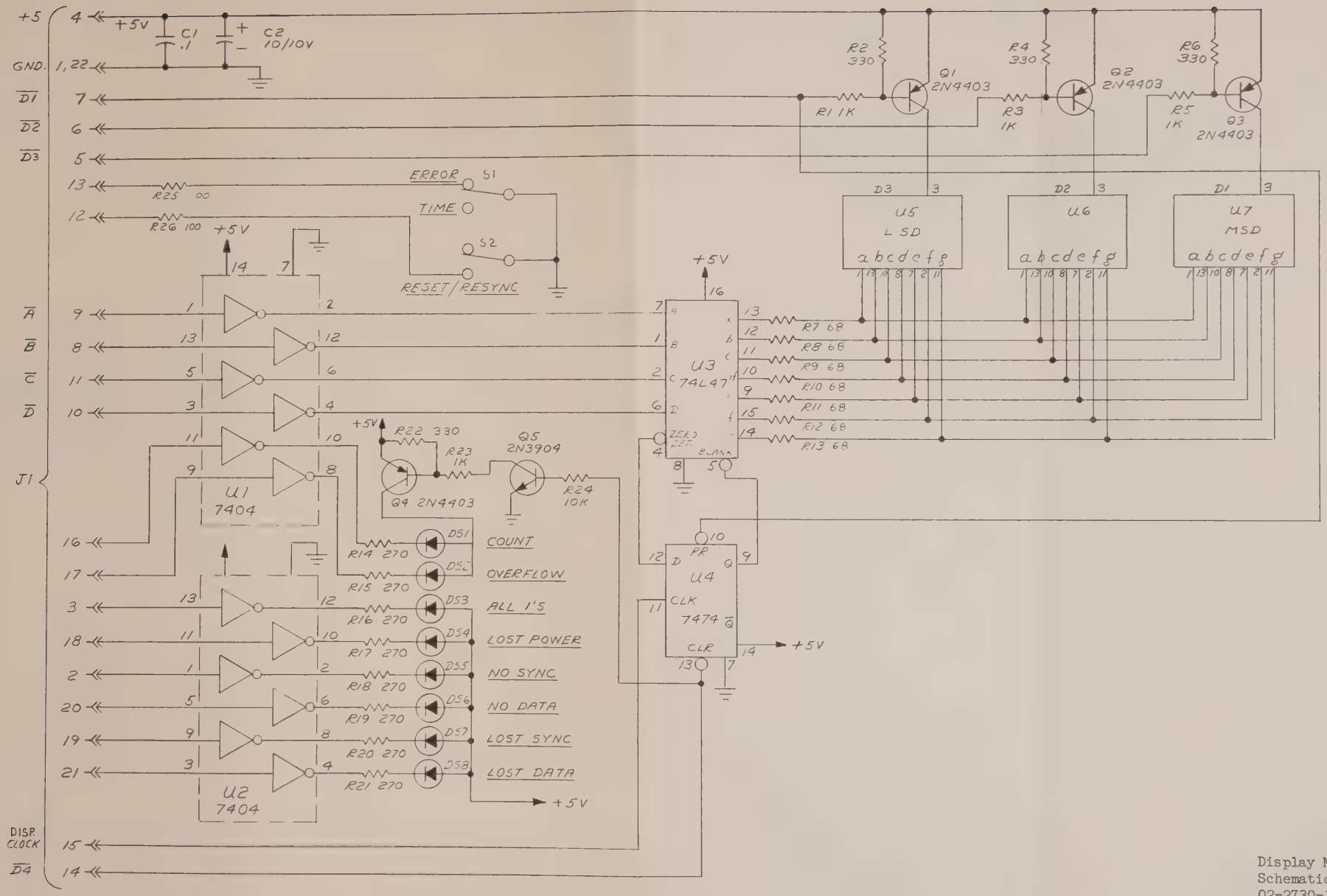
5.3.3 Receiver Checks

5.3.3.1 General Functional Check

(a) Perform the complete Self Test Procedure (See Section 2).

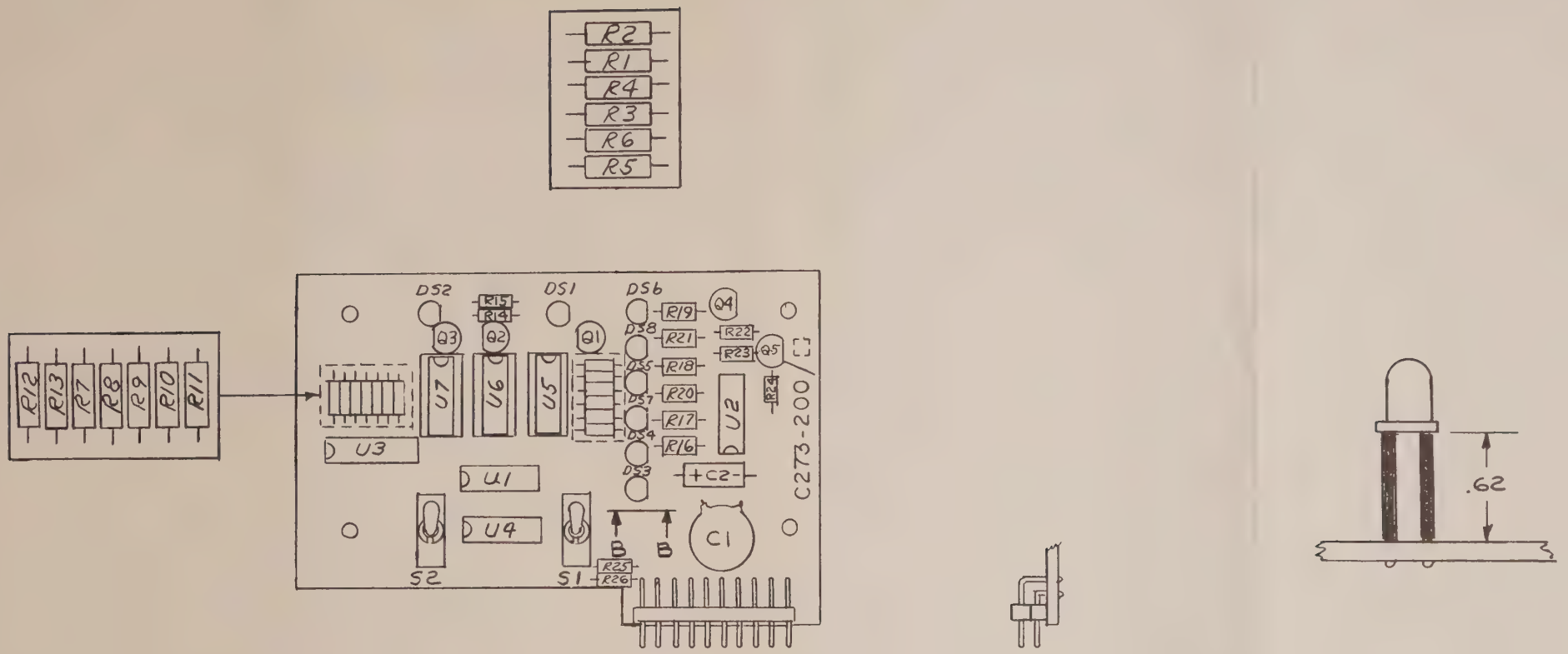
DIAGRAMS

FIGURE 1:	Display Module (A1) Schematic	02-2730-1000/C
FIGURE 2:	Display Module (A1) Assembly	02-2730-2300/M
FIGURE 3:	Interconnect Module (A2) Schematic	02-2730-1010/E
FIGURE 4:	Interconnect Module (A2) Assembly	02-2730-2010/D
FIGURE 5:	Receiver Module (A3) Schematic	02-2730-1190/C
FIGURE 6:	Receiver Module (A3) Assembly	02-2730-2190/C
FIGURE 7:	Transmitter Module (A4) Schematic (2 Sheets)	02-2730-1130/B
FIGURE 8:	Transmitter Module (A4) Assembly	02-2730-2130/A
FIGURE 9:	Receiver Logic Module (A5) Schematic	02-2730-1140/A
FIGURE 10:	Receiver Logic Module (A5) Assembly	[illegible]
FIGURE 11:	Power Supply Module (A6) Schematic	02-2730-1050/F
FIGURE 12:	Power Supply Module (A6) Assembly	02-2730-2050/C
FIGURE 13:	Buffer/APS Module (A7) Schematic (2 Sheets)	02-2730-1060/G
FIGURE 14:	Buffer/APS Module (A7) Assembly	02-2730-2060/F
FIGURE 15:	Display Logic (A8) Schematic	02-2730-1170/A
FIGURE 16:	Display Logic (A8) Assembly	02-2730-2170/A
FIGURE 17:	Receiver Reference Module (A10) Schematic	02-2730-1100/F
FIGURE 18:	Receiver Reference Module (A10) Assembly	02-2730-2100/L
FIGURE 19:	Digital Carrier Analysis Test Set Assembly	02-2730-2310/C



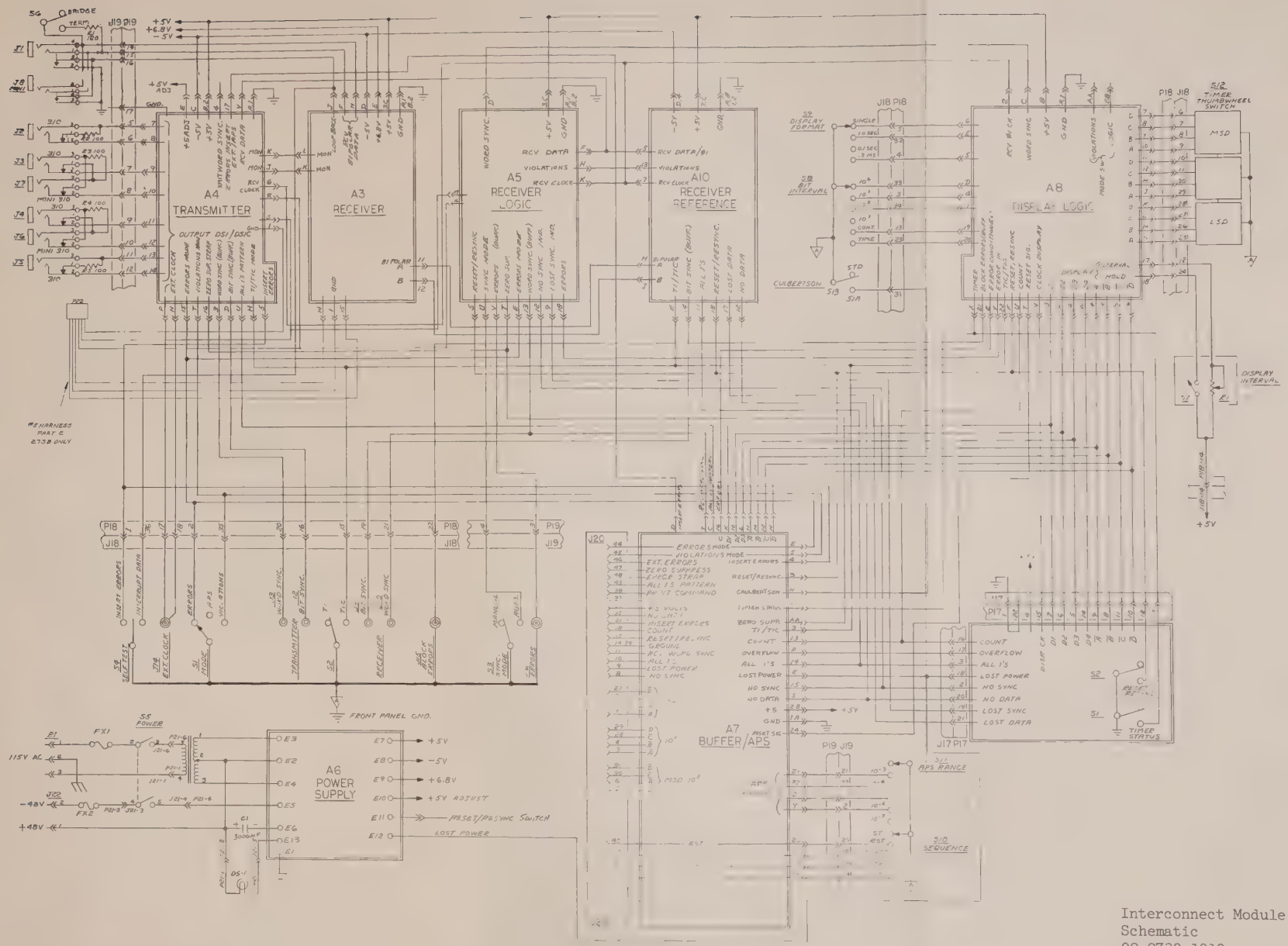
Display Module (A1)
Schematic
02-2730-1000

FIGURE 1



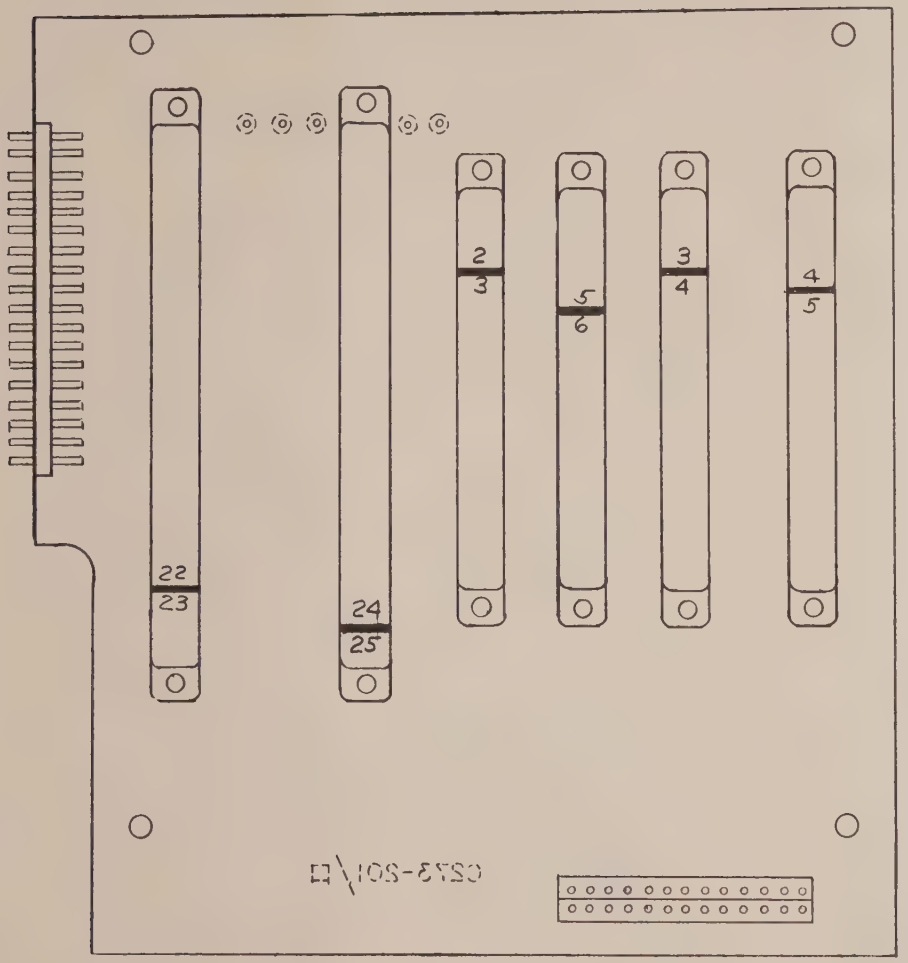
Display Module (A1)
Assembly
02-2730-2300

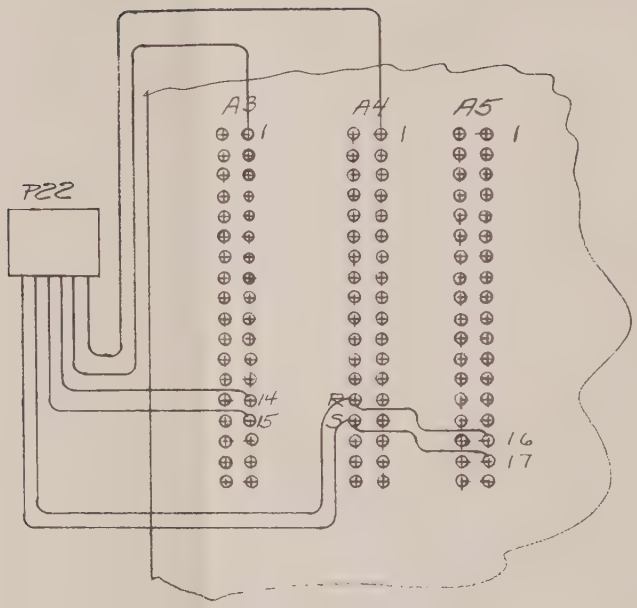
FIGURE 2



Interconnect Module (A2)
Schematic
02-2730-1010

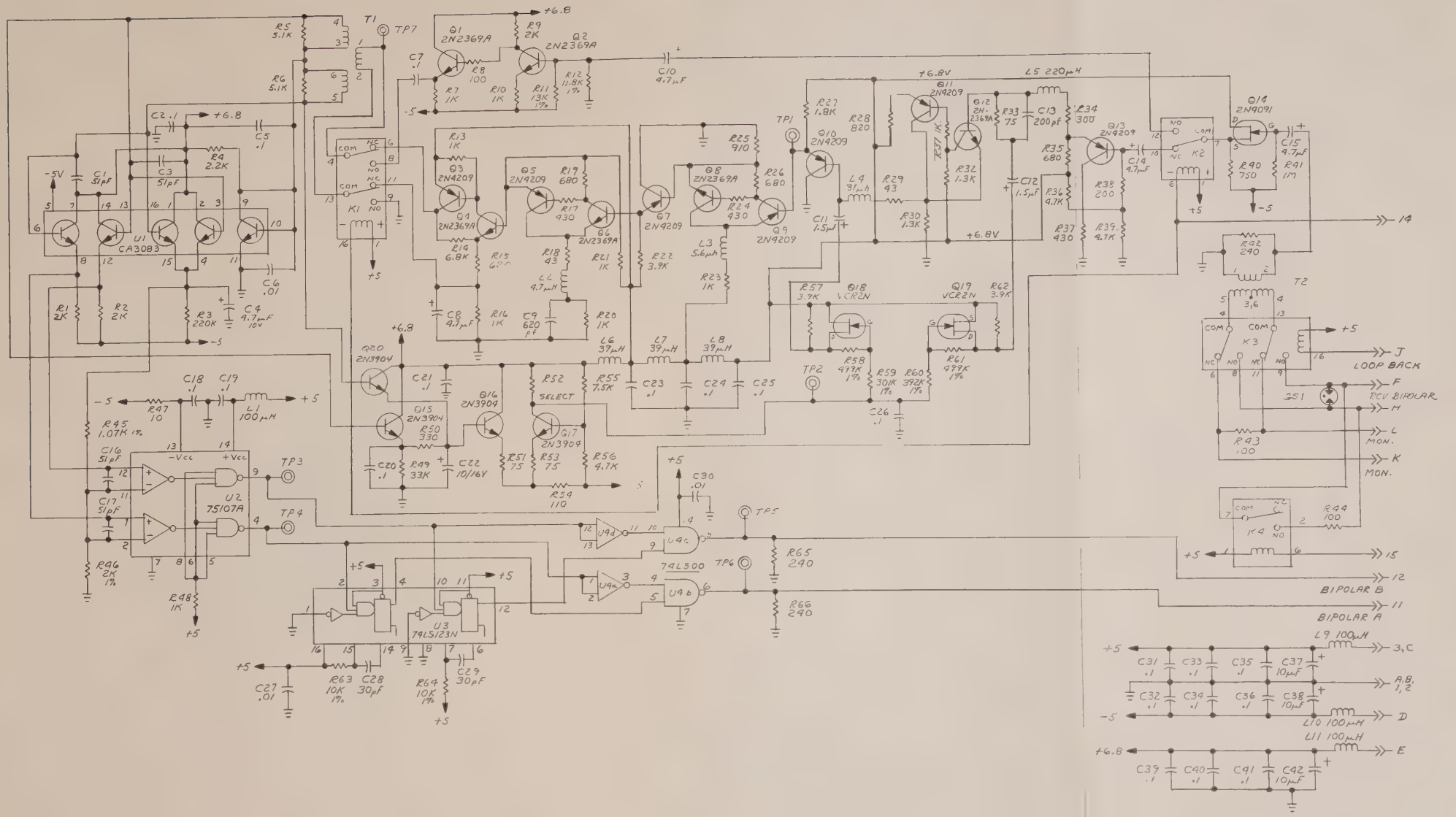
FIGURE 3





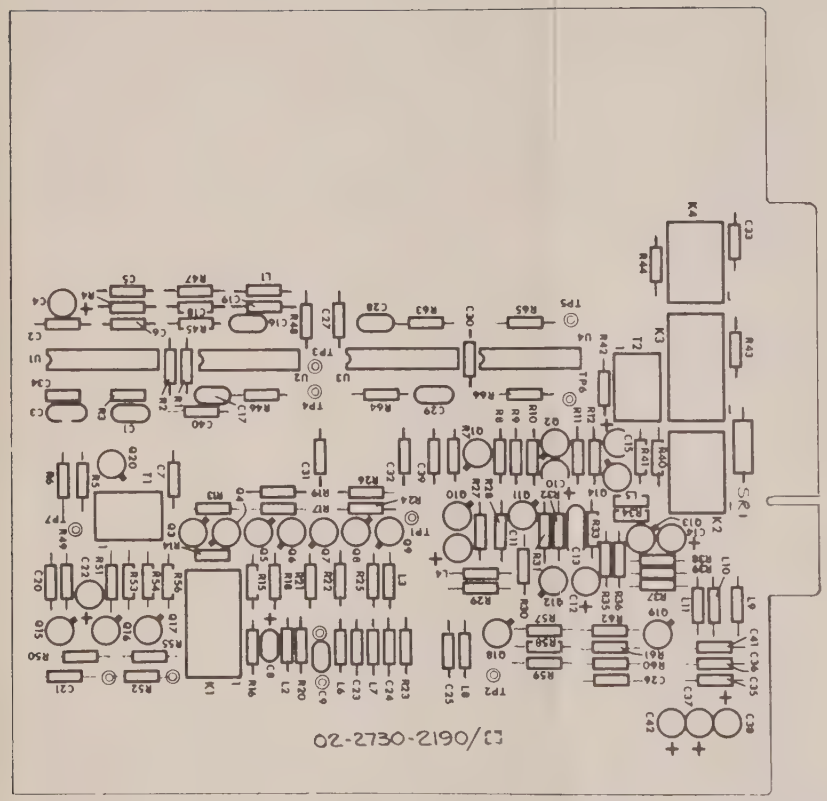
Interconnect Module (A2)
Assembly
02-2730-2010

FIGURE 4



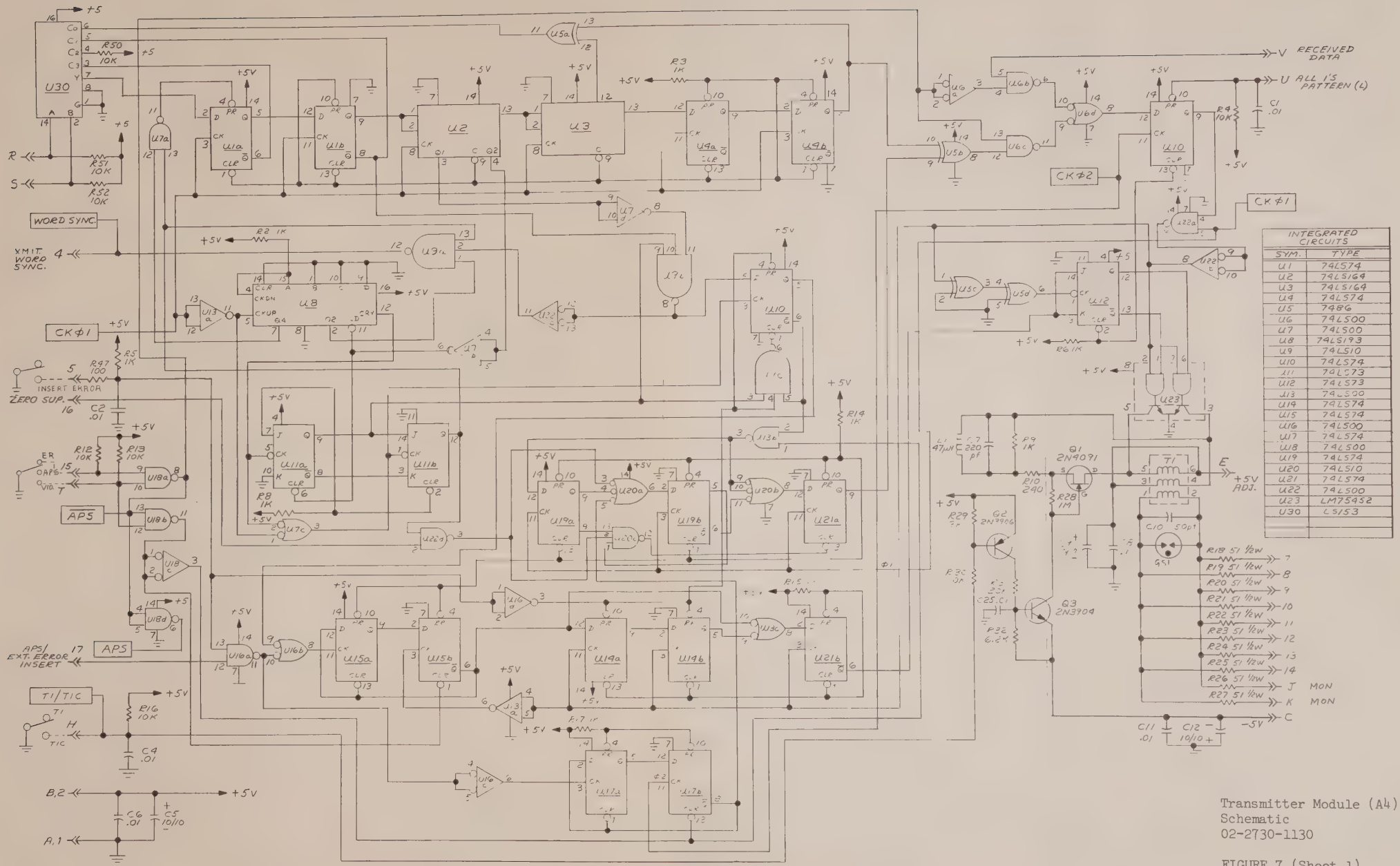
Receiver Module (A3)
Schematic
02-2730-1190

FIGURE 5



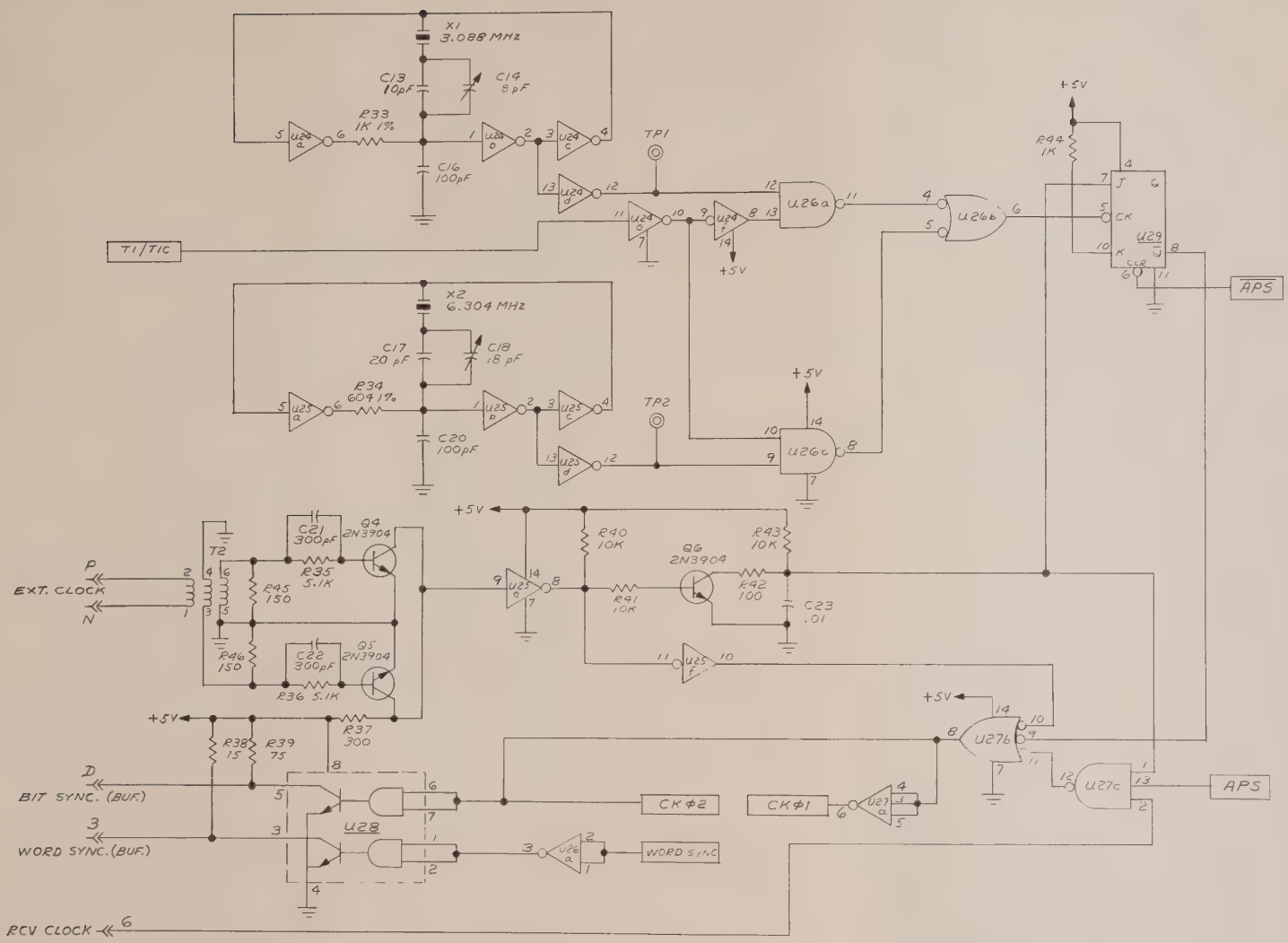
Receiver Module (A3)
Assembly
02-2730-2190

FIGURE 6



Transmitter Module (A4)
Schematic
02-2730-1130

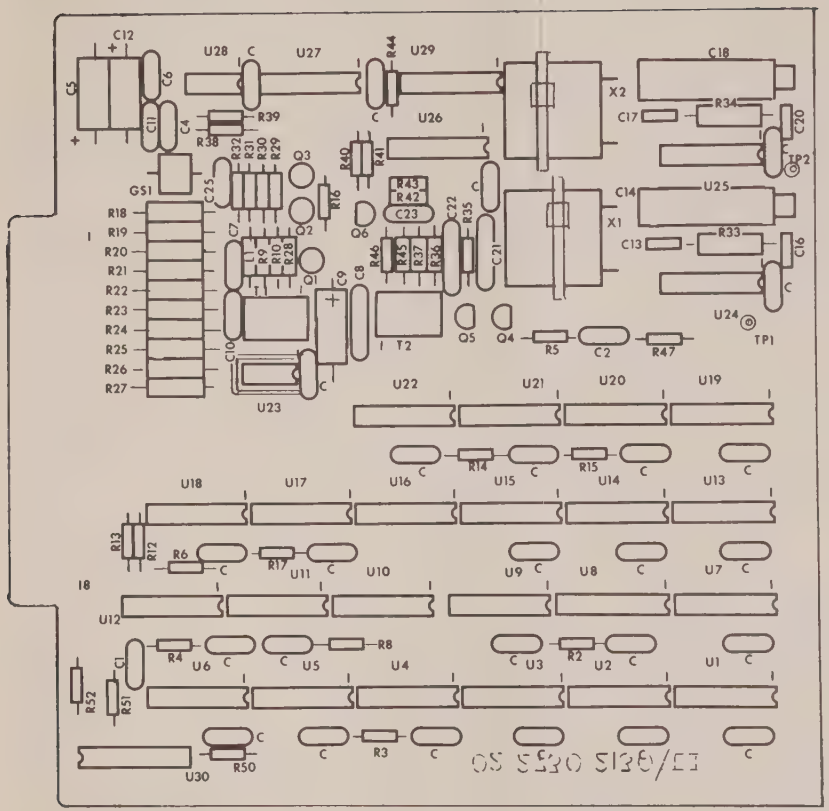
FIGURE 7 (Sheet 1)



INTEGRATED CIRCUITS	
SYM	TYPE
U24	7404N
U25	74S04
U26	74LS00
U27	74LS10
U28	75452
U29	74LS73

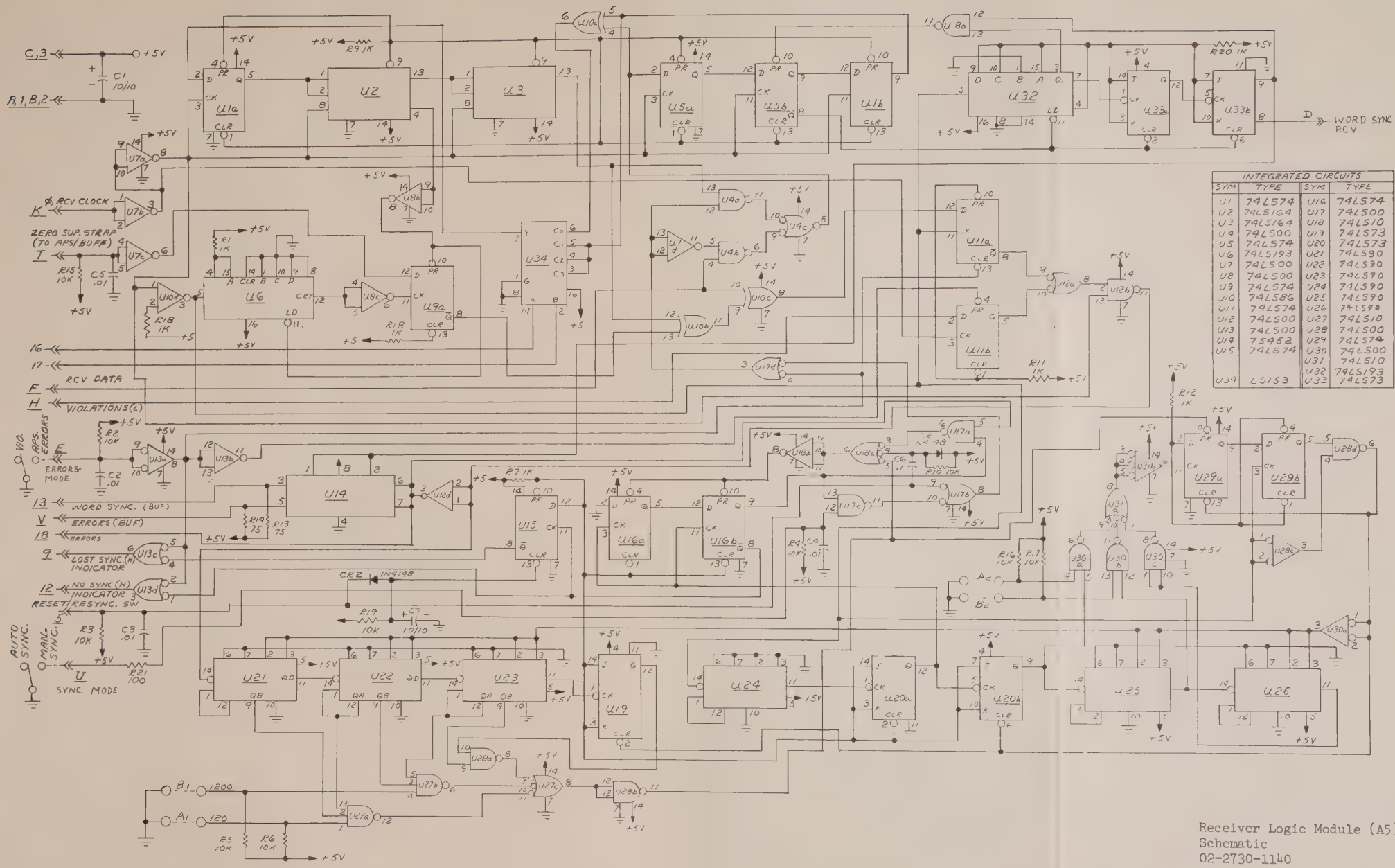
Transmitter Module (A4)
Schematic
02-2730-1130

FIGURE 7 (Sheet 2)



Transmitter Module (A4)
Assembly
02-2730-2130

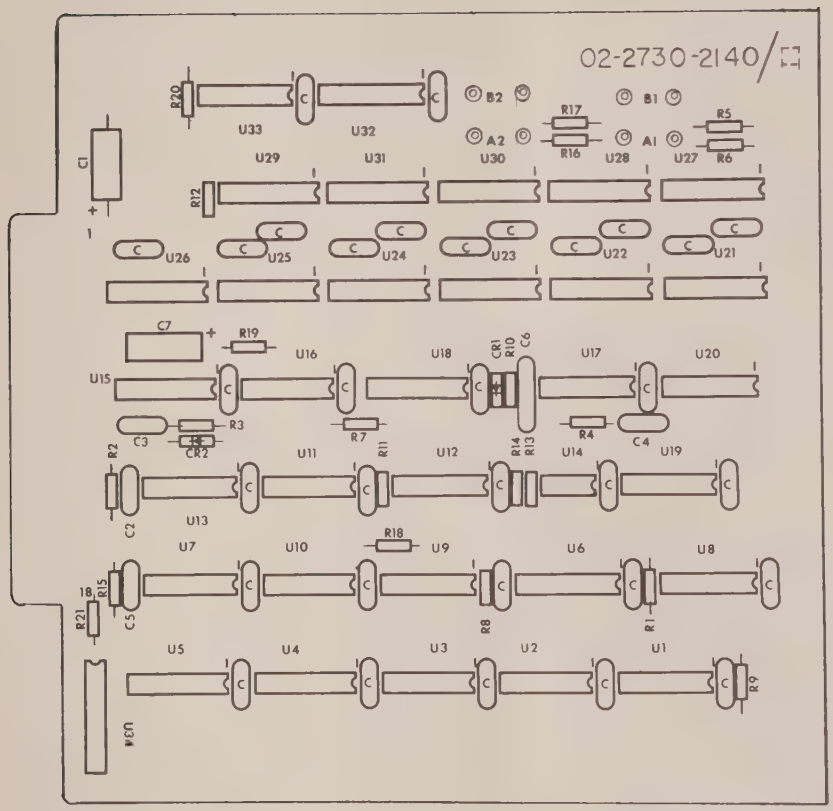
FIGURE 8



INTEGRATED CIRCUITS			
SYM	TYPE	SYM	TYPE
U1	74LS74	U16	74LS74
U2	74LS164	U17	74LS00
U3	74LS164	U18	74LS10
U4	74L500	U19	74LS73
U5	74LS74	U20	74LS73
U6	74LS193	U21	74LS90
U7	74LS00	U22	74LS90
U8	74LS00	U23	74LS90
U9	74LS74	U24	74LS90
U10	74LS86	U25	74LS90
U11	74LS74	U26	74LS90
U12	74LS00	U27	74LS10
U13	74LS00	U28	74LS00
U14	75452	U29	74LS74
U15	74LS74	U30	74LS00
		U31	74LS10
		U32	74LS193
U34	LS153	U33	74LS73

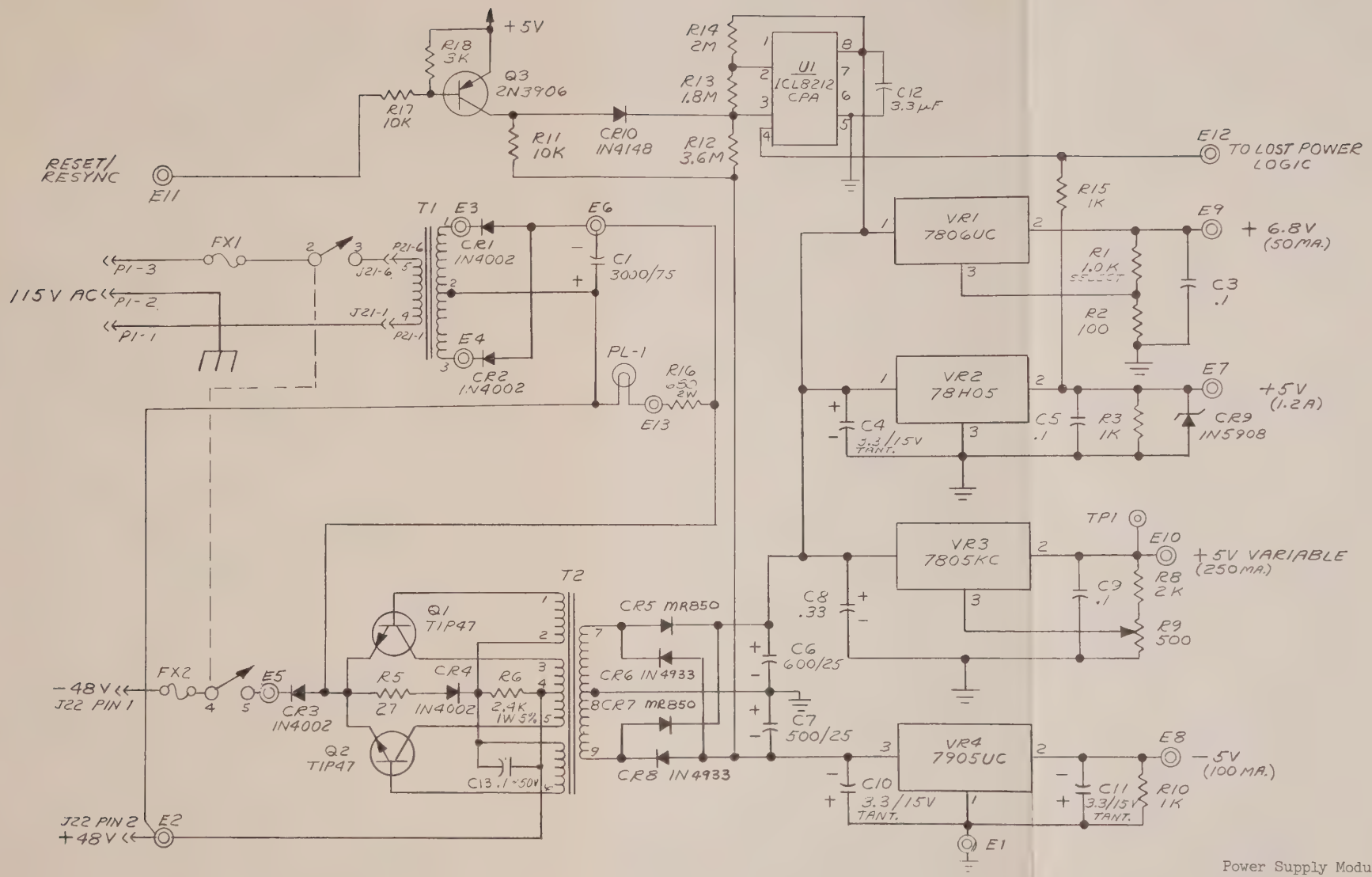
Receiver Logic Module (A5)
Schematic
02-2730-1140

FIGURE 9



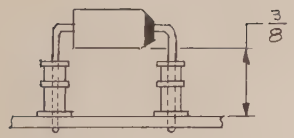
Receiver Logic Module (A5)
Assembly
02-2730-2140

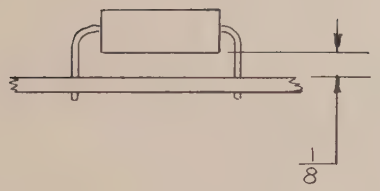
FIGURE 10

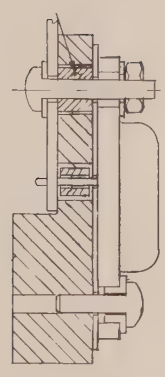


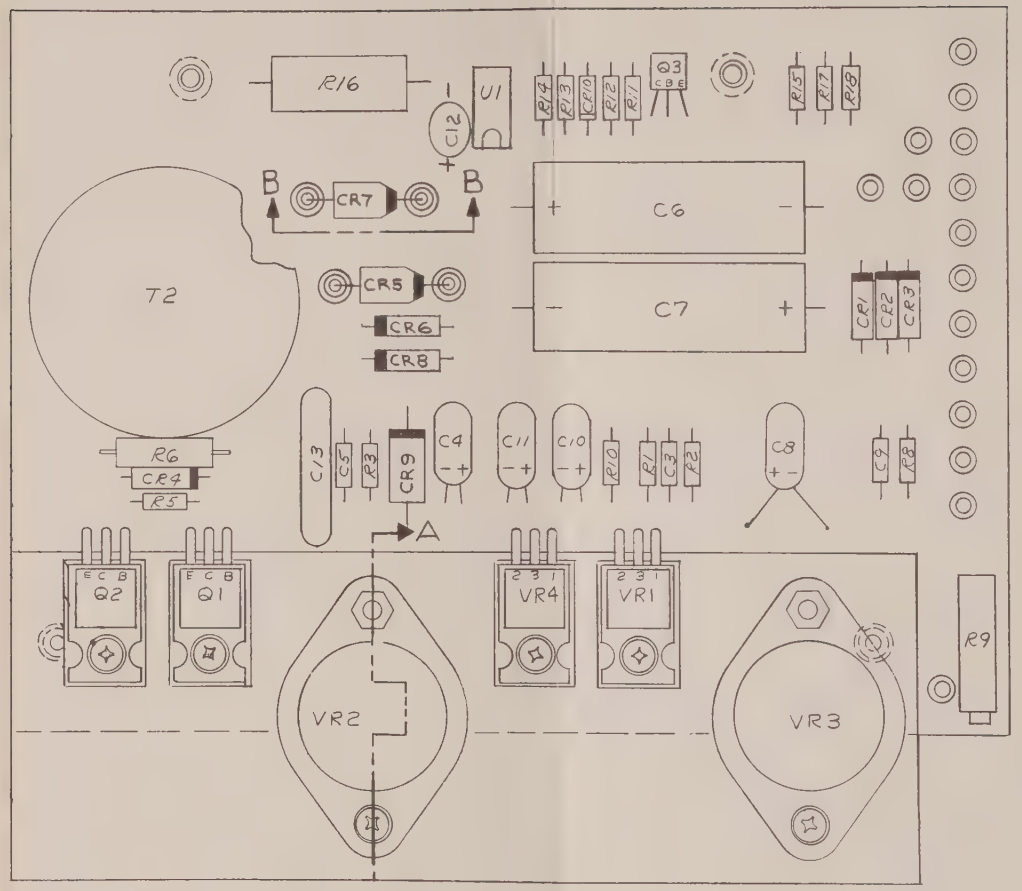
Power Supply Module (A6)
Schematic
02-2730-1050

FIGURE 11



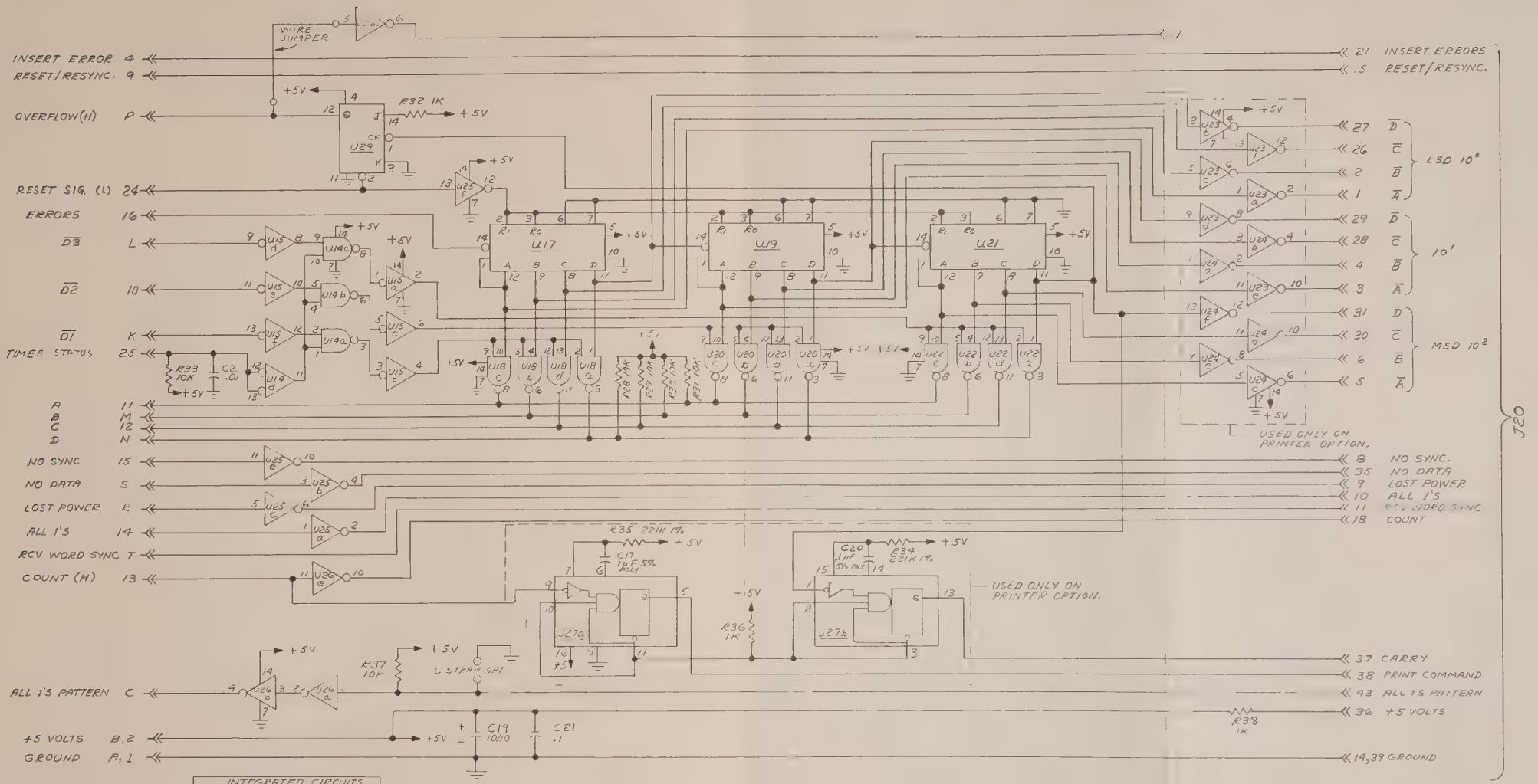






Power Supply Module (A6)
Assembly
02-2730-2050

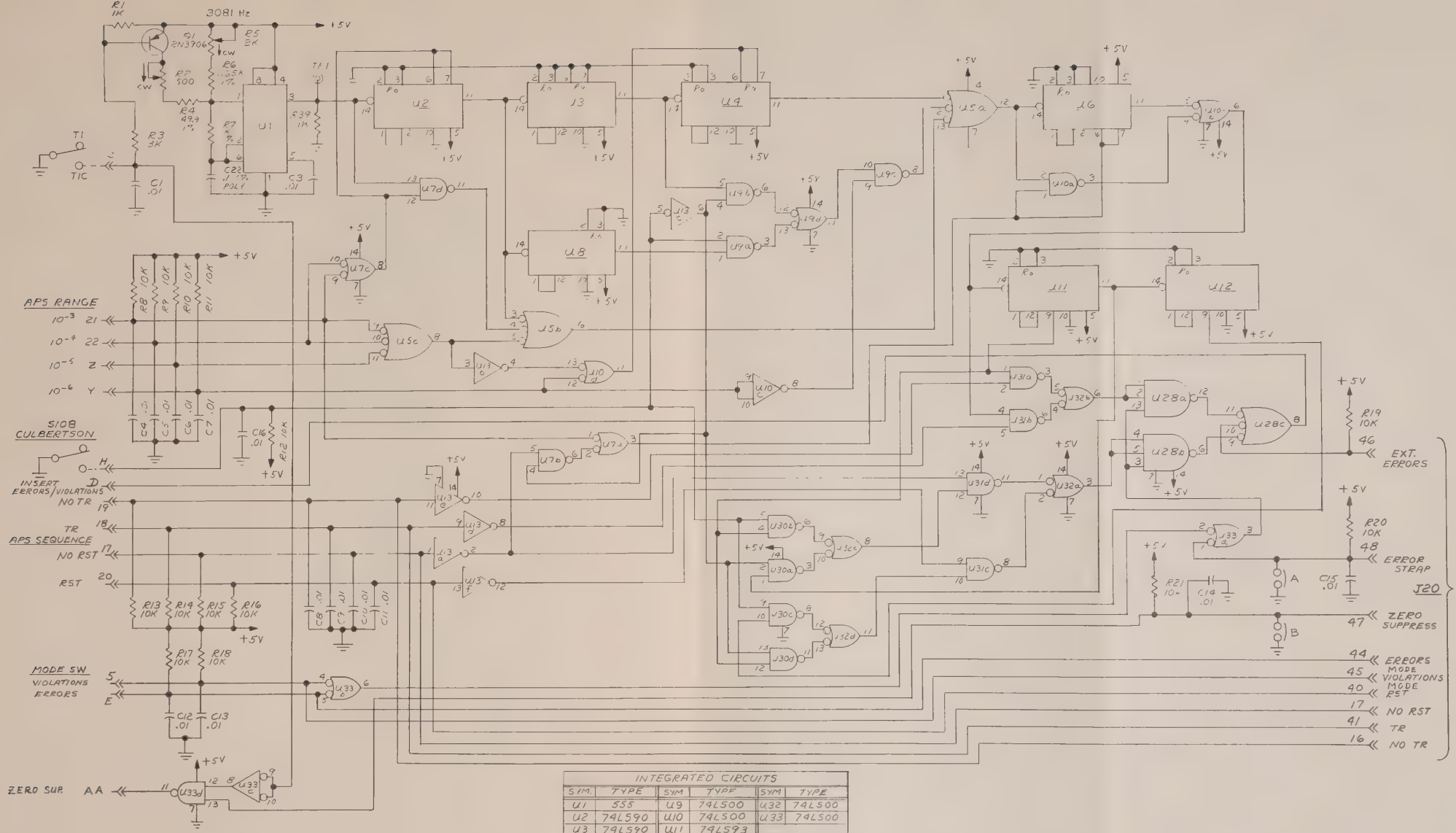
FIGURE 12



INTEGRATED CIRCUITS			
SYM.	TYPE	SYM.	TYPE
U19	74LS00	U26	74LS04
U15	74LS04	U27	74LS123
U16	74LS74	U29	74LS73
U17	74LS90		
U18	74LS03		
U19	74LS90		
U20	74LS03		
U21	74LS90		
U22	74LS03		
U23	74LS04		
U24	74LS04		
U25	74LS04		

Buffer/APS Module (A7)
Schematic
02-2730-1060

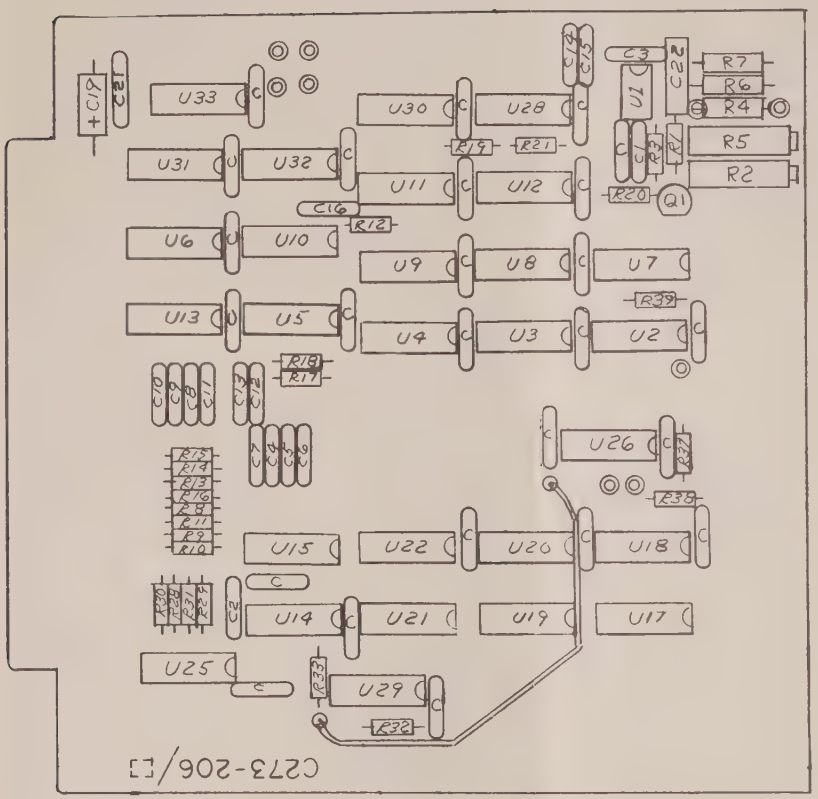
FIGURE 13 (Sheet 1)



INTEGRATED CIRCUITS					
SYM.	TYPE	SYM	TYPE	SYM	TYPE
U1	555	U9	74LS00	U32	74LS00
U2	74LS90	U10	74LS00	U33	74LS00
U3	74LS90	U11	74LS93		
U4	74LS90	U12	74LS93		
U5	74LS10	U13	74LS04		
U6	74LS90	U28	74LS10		
U7	74LS00	U30	74LS00		
U8	74LS93	U31	74LS00		

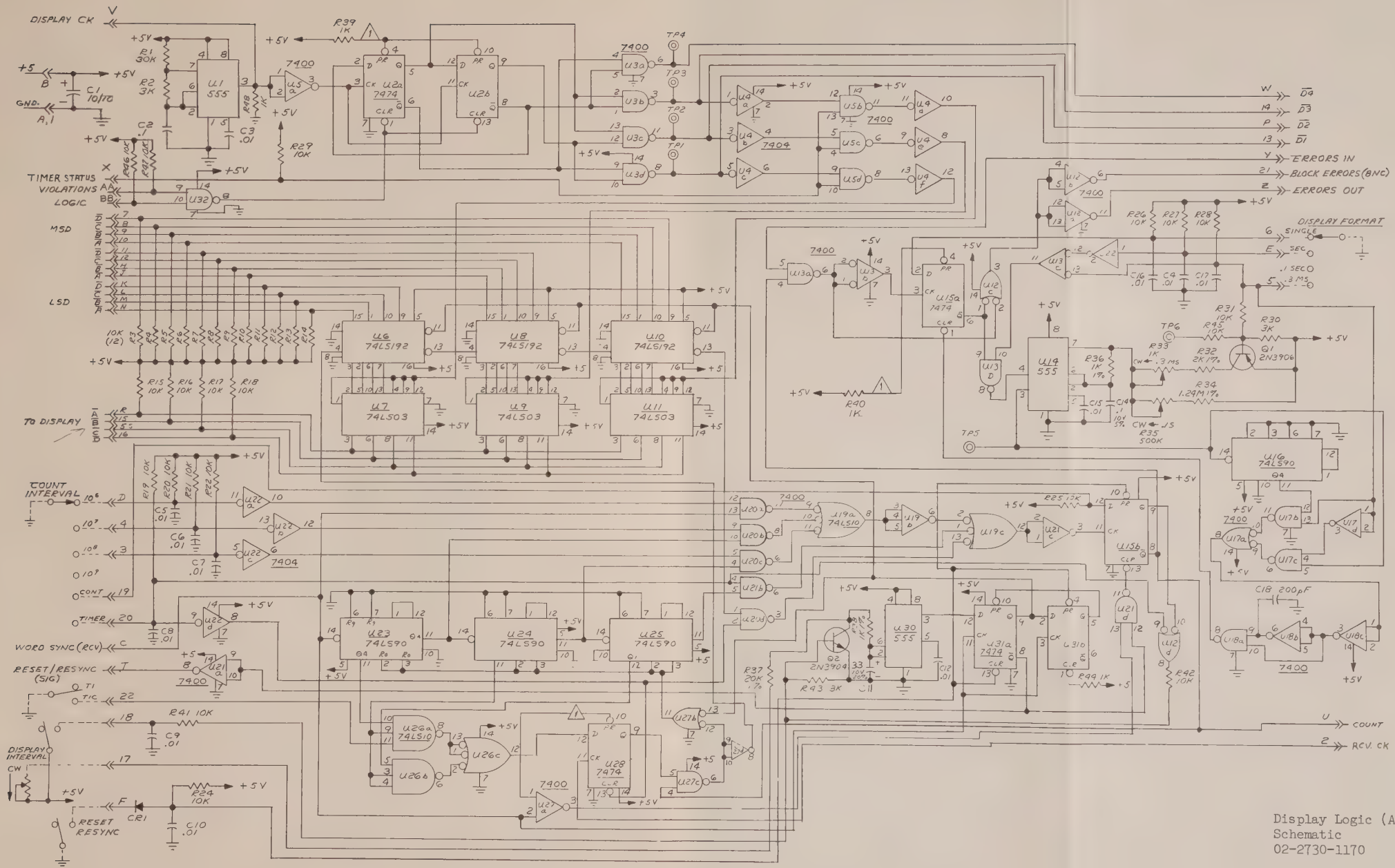
Buffer/APS Module (A7)
Schematic
02-2730-1060

FIGURE 13 (Sheet 2)



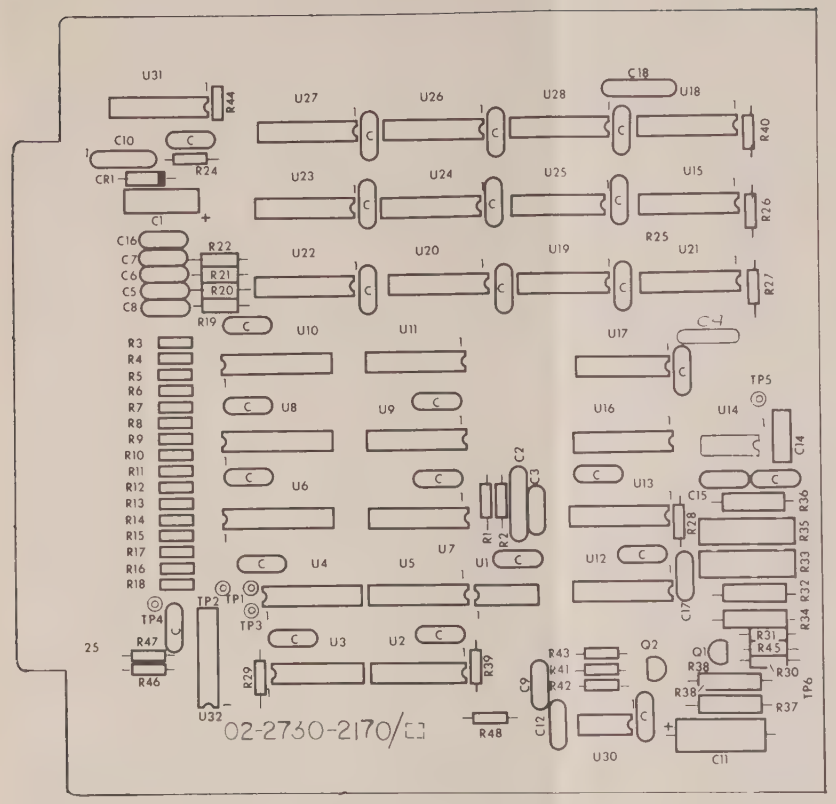
Buffer/APS Module (A7)
Assembly
02-2730-2060

FIGURE 14



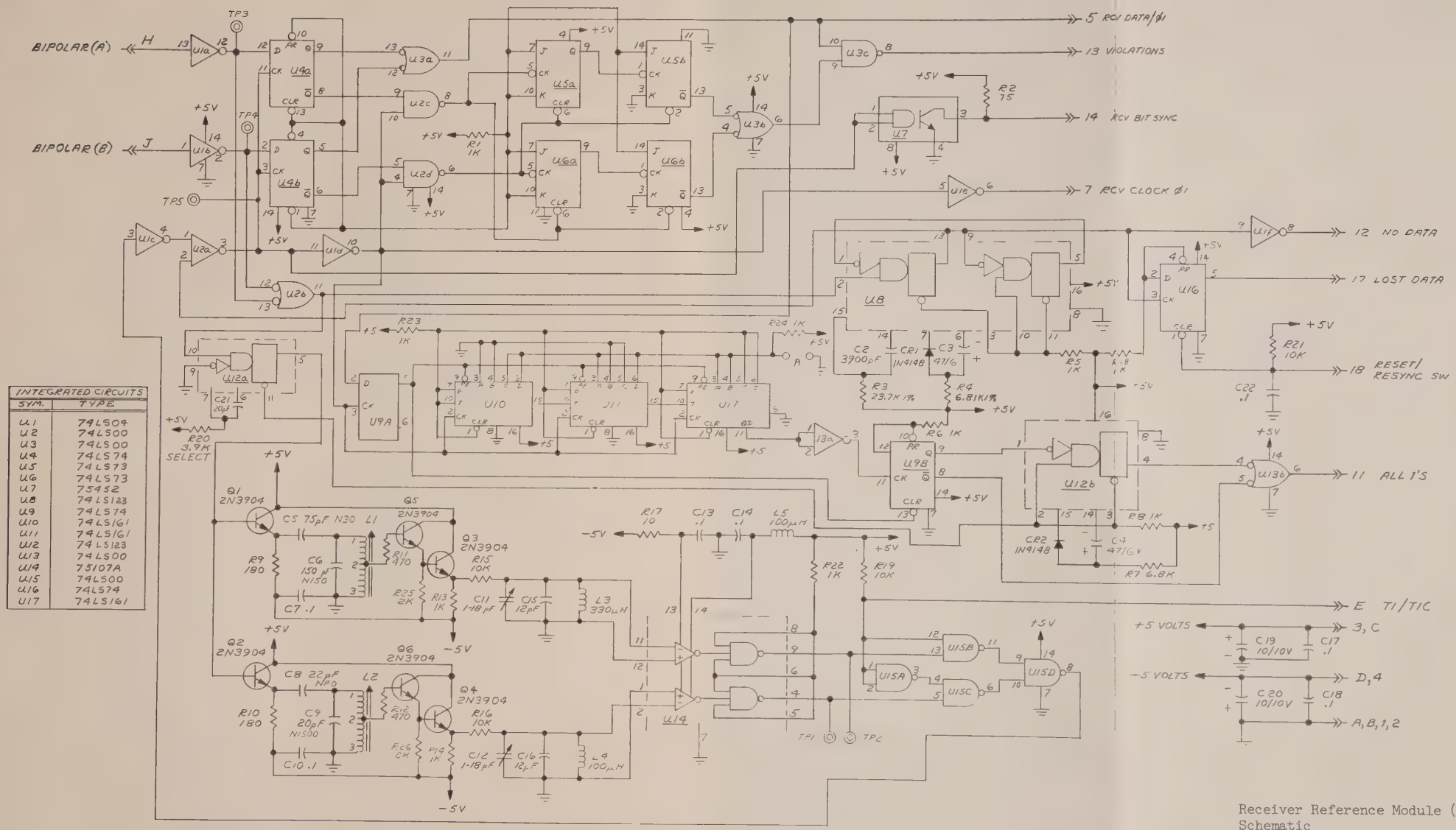
Display Logic (A8)
Schematic
02-2730-1170

FIGURE 15



Display Logic (A8)
Assembly
02-2730-2170

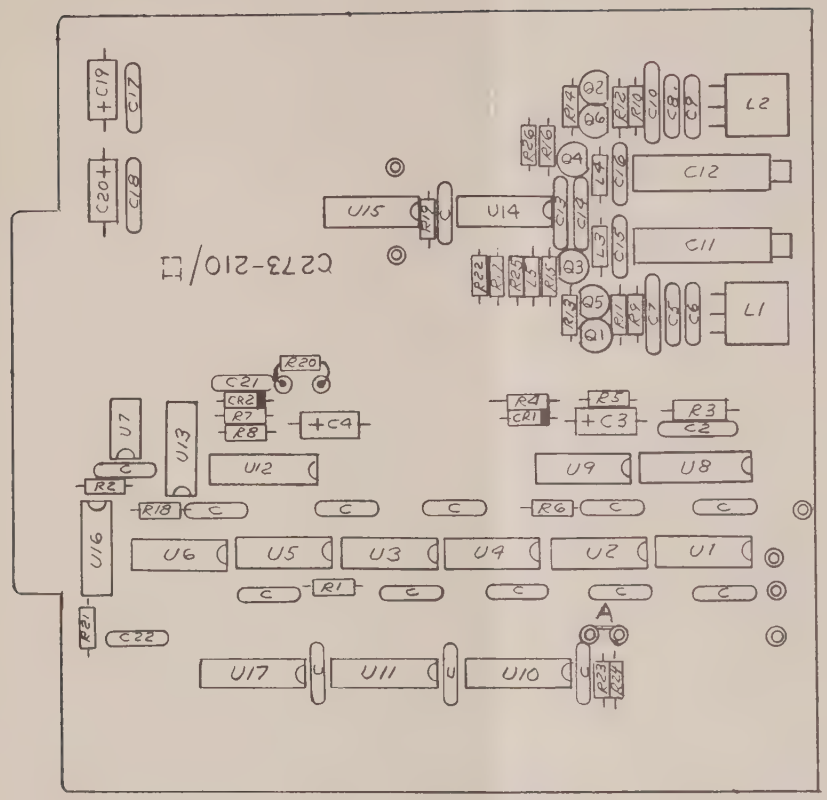
FIGURE 16



INTEGRATED CIRCUITS	
SYM.	TYPE
U1	74LS04
U2	74LS00
U3	74LS00
U4	74LS74
U5	74LS73
U6	74LS73
U7	75452
U8	74LS123
U9	74LS74
U10	74LS161
U11	74LS161
U12	74LS123
U13	74LS00
U14	75107A
U15	74LS00
U16	74LS74
U17	74LS161

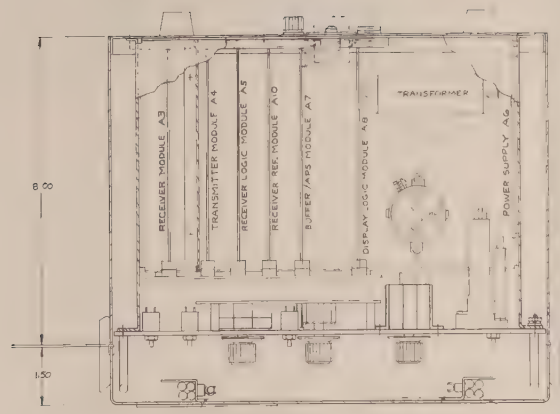
Receiver Reference Module (A10)
Schematic
02-2730-1100

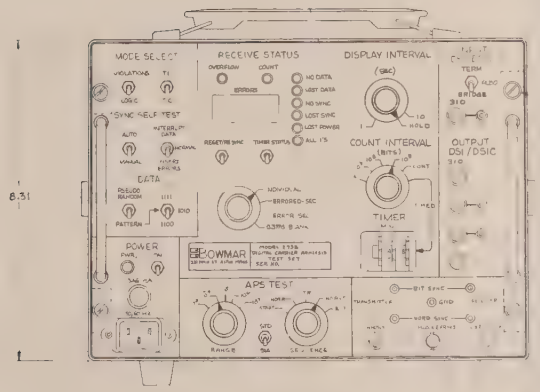
FIGURE 17



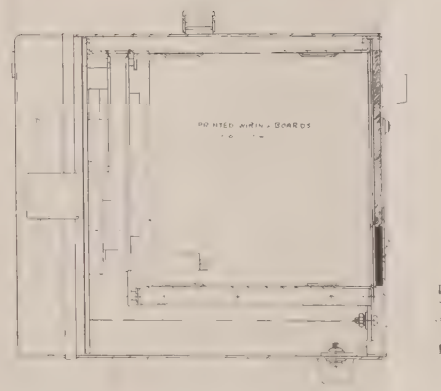
Receiver Reference Module (A10)
Assembly
02-2730-2100

FIGURE 18





SHOWN WITHOUT COVER



Digital Carrier Analysis
Test Set Assembly
02-2730-2310

FIGURE 19

PARTS AND MANUFACTURERS

Items listed herein are electrical and circuit components. They are grouped under the title of associated modules. Each part is itemized by REF. DES. (Reference Designation) and described according to title, values, manufacturer, and manufacturer's identification number. Exception to providing manufacturer identification is taken where the part is standardized RETMA. Any manufacturer registered for RETMA parts will be acceptable.

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
DISPLAY MODULE (A1)			
U1, 2	Inverter	T.I.	SN75LS04N
U3	Decoder 7-Seg. (BCD)	T.I.	SN74LS47N
U4	D-Type Flip Flop	T.I.	SN74LS74AN
U5, 6, 7	LED 7-Seg. Display	H.P.	5082-7650
DC1-8	LED Indicator	H.P	HLMP3300
Q1-4	Transistor		2N4403
R2, 3, 5, 22	Resistor, 330, 1/4W, 5%		RCR07G331JS
R1, 4, 5, 21	Resistor, 1K, 1/4W, 5%		RCR07G102JS
R7-13	Resistor, 68, 1/4W, 5%		RCR07G680JS
R14-21	Resistor, 270, 1/4W, 5%		RCR07G271JS
SC-2	PC Mount None-On-(On)	C&K	7109SPV30CQE
C1	Capacitor, .1µf, 20V Disc.	Centralab	UK-16-104
C2	Capacitor, 10µf, 16V, El.	Sprague	TE-1155E
Q5	Transistor		2N3904
R24	Resistor, 10K, 1/4W, 5%		RCR07G103JS
R25	Resistor, 100 ohm, 1/4W, 5%		RCR07G101JS
R26	Resistor, 10 ohm, 1/4W, 5%		RCR07G100JS
RECEIVER MODULE (A3)			
R1, 2, 9	Resistor, 2K, 1/4W, 5%		RCR07G202JS
R3	Resistor, 220K, 1/4W, 5%		RCR07G224JS
R4	Resistor, 2.2K, 1/4W, 5%		RCR07G222JS
R5, 6	Resistor, 5.1K, 1/4W, 5%		RCR07G512JS
R13,20,21,23,7, R10,48,31,16	Resistor, 1.0K, 1/4W, 5%		RCR07G102JS
R8, 43, 44	Resistor, 100, 1/4W, 5%		RCR07G101JS
R11	Resistor, 13.0K, 1/8W, 1%		RN55C1302F
R12	Resistor, 11.8K, 1/8W, 1%		RN55C1182F
R14	Resistor, 6.8K, 1/4W, 5%		RCR07G682JS
R15	Resistor, 650, 1/4W, 5%		RCR07G651JS
R17, 24, 37	Resistor, 430, 1/4W, 5%		RCR07G431JS
R18, 29	Resistor, 43, 1/4W, 5%		RCR07G430JS
R19, 26, 35	Resistor, 680, 1/4W, 5%		RCR07G681JS
R22, 57, 62	Resistor, 3.9K, 1/4W, 5%		RCR07G392JS

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
[illegible]			
R5	Resistor, 910, 1/4W, 5%		RCR07G911JS
R7	Resistor, 1.8K, 1/4W, 5%		RCR07G182JS
R9	Resistor, 820, 1/4W, 5%		RCR07G821JS
R10, 12	Resistor, 1.3K, 1/4W, 5%		[illegible]
R11, 13, 15	Resistor, 75, 1/4W, 5%		RCR07G750JS
R16	Resistor, 300, 1/4W, 5%		RCR07G301JS
R17, 18, 19	Resistor, 4.7K, 1/4W, 5%		[illegible]
R20	Resistor, 200, 1/4W, 5%		RCR07G201JS
R21	Resistor, 750, 1/4W, 5%		RCR07G751JS
R22	Resistor, 1M, 1/4W, 5%		RCR07G105JS
R23, 24, 25	Resistor, 240, 1/4W, 5%		RCR07G241JS
R26	Resistor, 1.07K, 1/8W, 1%		RN55C1071F
R27	Resistor, 2.0K, 1/8W, 1%		RN55C2001F
R28	Resistor, 10, 1/4W, 5%		RCR07G100JS
R29	Resistor, 33K, 1/4W, 5%		RCR07G333JS
R30	Resistor, 330, 1/4W, 5%		RCR07G331JS
R31	Resistor, 110, 1/4W, 5%		RCR07G111JS
R32	Resistor, 7.5K, 1/4W, 5%		RCR07G752JF
R33, 41	Resistor, 499K, 1/8W, 1%		RN55C4993F
R34	Resistor, 301K, 1/8W, 1%		RN55C3013F
R36	Resistor, 392K, 1/8W, 1%		RN55C3923F
R37, 44	Resistor, 10.0K, 1/8W, 1%		RN55C1002F
R38	Resistor, 3.9K, 1/4W, 5% (Select)		[illegible]
C1,3,12,17	Capacitor, 51pf, 5%	CDE	CD10ED510J03
C2,5,7,[illegible],19,21,23, C24,[illegible],29,30,34,35, C36,40,41,31,32,33, C39	Capacitor, 0.1uf, 50V	Unitrode	CGC103ZDZ
C4,8,10,14,15	Capacitor, 4.7uf, 10V	Sprague	196D475X9010HA1
C6, 27, 30	Capacitor, .01uf, 50V	Unitrode	CGD104ZDZ
C9	Capacitor, 620pf, 500V, 5%	CDE	[illegible]
C11, 16	Capacitor, 1.5uf, 25V	Sprague	196D155X9025HA1

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
C13	Capacitor, 200pf, 500V, 5%	CDE	CM04FD201J03
C[illegible]	Capacitor, 10µf, 20V	Sprague	196D106X9020JA1
C28, 29	Capacitor, 30pf	CDE	CM04ED300J03
U1	Integrated Circuit	RCA	CA3083E
U2	Integrated Circuit	T.I.	SN75107AN
U3	Integrated Circuit		75LS123N
U4	Integrated Circuit		75LS00N
Q1,2,4,6,8,12	Transistor, NPN		2N2369A
Q3,5,7,9,10,11,13	Transistor, PNP		2N4209
Q14	Transistor, FET		2N4091
Q15,16,17,20	Transistor, NPN		2N3904
Q18, 19	Transistor, FET		VCR2N
SR1	Transient Suppressor	Clare	CG90L
L1,9,10,11	Inductor, 100µh	Lenox Fugle	NR-100, LF-100
L2	Inductor, 4.7µh	Lenox Fugle	NR-4.7, LF-4.7
L3	Inductor, 5.6µh	Lenox Fugle	NR-5.6, LF-5.6
L4	Inductor, 31µh	Lenox Fugle	NR-31, LF-31
L5	Inductor, 220µh	Lenox Fugle	NR-220, LF-220
L6, 7, 8	Inductor, 39µh	Lenox Fugle	NR-39, LF-39
T1, 2	Transformer	Pulse Engineering	PE-5763
K1, 3	Relay, 2C	Aromat	DS2E-M-DC5V
K2, 4	Relay, 1C	Aromat	DS1E-M-DC5V
TRANSMITTER MODULE (A4)			
U1,4,10,14.15,17,19,21	D Type Flip Flop	T.I.	SN74LS74AN
U2, 3	8 Bit shift Register	T.I.	SN74LS164N
U5	Exclusive OR	T.I.	SN74LS86AN
U6,7,13,16,18,22,26	Quad 2 Input NAND	T.I.	SN74LS00N
U8	4 Bit Up/Down Counter	T.I.	SN74LS193N
U9, 20, 27	Triple 3 Input NAND	T.I.	SN74LS10N

REF. DES.	COMPONENT DESCRIPTION	[illegible]	PART NO.
TRANSMITTER MODULE (A4) (Con't)			
U12, 29, 11	JK Flip Flop	T.I.	SN74LS73N
U23, 28	Line Driver	T.I.	SN75452BP
U25, 24	Hex Inverter	T.I.	SN74LS04N
Q1	FET		2N4091
Q2	PNP Transistor		2N3906
Q3,4,5,6	NPN Transistor		2N3904
U30	4-1 MUX	T.I.	SN75LS153N
X1	3.088 MC Xtal Crystal	[illegible]	B6440
X2	6.034 MC Xtal Crystal	[illegible]	B6441
R2,3,5,6,8,9,14,15,17,44	Resistor, 1K, 5%, 1/4W		RCR07G102JS
R4,12,14,16,30,40,41,43, R50, 51, 52	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R10	Resistor, 240, 5%, 1/4W		RCR07G241JS
R18-27	Resistor, 51, 5%, 1/2W		RCR20G510JS
R28	Resistor, 1M, 5%, 1/4W		RCR07G105JS
R29	Resistor, 3K, 5%, 1/4W		RCR07G302JS
R31	Resistor, 20K, 5%, 1/4W		RCR07G203JS
R32	Resistor, 6.2K, 5%, 1/4W		RCR07G622JS
R33	Resistor, 1K, 1%, 1/8W		RN60C1001F
R35, 36	Resistor, 5.1K, 5%, 1/4W		RCR07G512JS
R37	Resistor, 300, 5%, 1/4W		RCR07G301JS
R42, 47	Resistor, 100, 5%, 1/4W		RCR07G101JS
R45, 46	Resistor, 150, 5%, 1/4W		RCR07G151JS
C1,2,4,6,11,23,25	Capacitor, .01µf, Disc.	[illegible]	UK-16-103
C5,9,12	Capacitor, 10µf, 16V, Tant.	Sprague	TE-1155E
C7	Capacitor, 220pf, Silver Mica	CDE	CD10FD221J03
C8	Capacitor, .1µf	[illegible]	UK-16-104
C10	Capacitor, 50pf, Silver Mica	CDE	CD10ED510J03
C13, 17	Capacitor, 10pf, 5%, N1500	[illegible]	CG10-NP0 5%
C14, 18	Capacitor, 1-10pf Adj.	[illegible]	GGC-10000
C16, 20	Capacitor, 100pf, Silver Mica	[illegible]	CD10FD101J03
C21, 22	Capacitor, 300pf, Silver Mica	[illegible]	CD10FC201J03
R38, 39	Resistor, 75, 5%, 1/4W		RCR07G750JS
T1, 2	Pulse Transformer, 200µh	Pulse Engineering	PE57653
L1	47µh Coil	Lenox Fugle	NR-47
VR1	Trancient Suppressor		CG70L
R39	Resistor, 604, 1%, 1/8W	[illegible]	[illegible]

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
RECEIVER LOGIC (A5)			
U1,5,9,11,15,16,29	D Type Flip Flop	T.I.	SN75LS75AN
U2, 3	Shift Register, 8 Bit	T.I.	SN74LS164AN
U4,7,8,12,13,17,28,30	Quad NAND	T.I.	SN74LS00N
U6, 32	Counter Binary Up/Down	T.I.	SN74LS193N
U[illegible]	4-1 MUX	T.I.	SN74LS153N
U[illegible]	Line Driver	T.I.	SN75452BP
U18, 27, 31	Triple 3 Input NAND	T.I.	SN74LS10N
U19, 20, 33	JK Type Flip Flop	T.I.	SN74LS73N
U21,22,23,24,25,26	Decade Counter	T.I.	SN74LS90N
R1, 7,8,9,11,12,18,20	Resistor, 1K, 5%, 1/4W		RCR07G102JS
R[illegible]	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R17, 19			
CR1, 2	Diode		1N4148
C[illegible]	Capacitor, 10µf	Sprague	TE-1155E
C2,3,4,5	Capacitor, .01µf, Disc.	Centralab	UK-16-103
C6	Capacitor, .1µf, Disc.	Centralab	UK-16-104
R14, 13	Resistor, 75, 5%, 1/4W		RCR07G750JS
U1C	Quad EX-OR		SN74LS86N
R21	Resistor, 100, 1/4W, 5%		RCR07G101JS
POWER SUPPLY MODULE (A6)			
VR1	6 VDC Reg. with Mica Insulator & Shoulder Washers	Fairchild	UA7806UC
VR2	5 VDC Reg. with Mica Insulator & Shoulder Washers	Fairchild	UA78H05SC
VR3	5 VDC Reg. with Mica Insulator & Shoulder Washers	Fairchild	UA7805KC
VR4	-5 VDC Reg. with Mica Insulator & Shoulder Washers	Fairchild	UA7905UC
CR1,2,3,4	Diode		1N4002
CR5, 7	Diode	Motorola	MR850
CR6, 8	Diode	Motorola	1N4933

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
POWER SUPPLY MODULE (A6) (Con't)			
Q1, 2	Power Transistor with Mica Insulator and Shoulder Washers	T.I.	TIP 47
[illegible]	Transistor		2N3906
CR9	Zener Diod[illegible]		1N5908
CR10	Diode		1N4148
T2	Transformer Converter SCD	Bowmar	C6447
IC1	IC	[illegible]	ICL8212CPA
R[illegible]	Resistor, 100, 5%, 1/4W		RCR07G101JS
R1, 3, 10, 15	Resistor, 1K, 5%, 1/4W		RCR07G102JS
[illegible]	Resistor, 27, 5%, 1/2W		RCR20G270JS
[illegible]	Resistor, 2.4K, 5%, 1W		RCR32G242JS
[illegible]	Resistor, 2K, 5%, 1/4W		RCR07G202JS
[illegible]	Potentiometer, 500 ohm	Beckman	89WR500
R11, 17	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R[illegible]	Resistor, 3.6M, 5%, 1/4W	Mepco/Electra	5043EM
R[illegible]	Resistor, 1.8M, 5%, 1/4W		RCR07G185JS
R[illegible]	Resistor, 2M, 5%, 1/4W		[illegible]
R[illegible]	Resistor, 680, 5%, 2W		RL42S681JTX
C[illegible]	Capacitor, .1µf		UK-16-104
C[illegible]	Capacitor, 3.3µf/15VDC Tant.		196D335X9015HA1
C[illegible]	Capacitor, .33µf/35VDC Tant.		196D334X9035HA1
C[illegible]	Capacitor, 600µf/25VDC		500D607G025FK7
C[illegible]	Capacitor, [illegible]		500D507G025FH7
J[illegible]	Terminals	Cambion	2027-2
R[illegible]	Resistor, 3K, 5%, 1/4W		RCR07G302JS
C[illegible]	Capacitor, .1µf @ 50V Disc.	Centralab	CK05BX104K
BUFFER/ATC MODULE			
U2,3,4,6,21,17,19	Decade Counter	T.I.	SN74LS90N
U5, 26	Triple 3 In. NAND	T.I.	SN74LS10N
U7,9,10,30,31,14,32,33	Quad 2 In. NAND	T.I.	SN74LS00N
U11, 12, 8	Bin Counter	T.I.	SN74LS93N

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
BUFFER/APS MODULE (Con't)			
U13,15,25,26	Hex Inverter	T.I.	SN74LS04N
U29	Dual JK-FF	T.I.	SN74LS73N
U1	Timer	National	LM555CN
C21	Capacitor, .1µf, Disc.	Centralab	UK-16-104
C1-16	Capacitor, .01µf, Disc.	Centralab	UK-16-103
C19	Capacitor, 10µf, 16V, EL	Sprague	TE-1155E
C22	Capacitor, 0.1µf, 5%, Poly.	Siemens	B32651-0.1/5/250
R28-31, 33, 8-21,37	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R32, 38, 1, 39	Resistor, 1K, 5%, 1/4W		RCR07G102JS
R3	Resistor, 3K, 5%, 1/4W		RCR07G302JS
R4	Resistor, 1.43K, 1%, 1/8W		RN60C1431F
R6	Resistor, 2.80K, 1%, 1/8W		RN60C2801F
R7	Resistor, 499K, 1%, 1/8W		RN60C4990F
R2	Potentiometer, 500 ohm	Beckman	89WR500
R5	Potentiometer, 2K	Beckman	89WR2K
Q1	Transistor, PNP	2N3906	
U18, 20, 22	Quad, Input NAND O.C.	T.I.	SN74LS03J
DISPLAY LOGIC (A8)			
U1, 14, 30	Timer	National	LM555CN
U2,15,28,31	D Type Flip Flop	T.I.	SN74LS74AN
U3,5,12,13,19,20,21, U27, 32, 18	Quad 2 Input NAND	T.I.	SN74LS00N
U4, 22	Hex Inverter	T.I.	SN74LS04N
U6, 8, 10	Counter Decade Up/Down	T.I.	SN74LS192N
U7, 9, 11	Quad 2 Input NAND O/C	T.I.	SN74LS03N
U16, 23, 24, 25	Counter BDC	T.I.	SN74LS90N
U19, 26	Triple 3 Input NAND	T.I.	SN74LS10N
Q1	Transistor, PNP	Motorola/ITT	2N3906
Q2	Transistor, NPN	Motorola/ITT	2N3904

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
DISPLAY LOGIC (A8) (Con't)			
R1	Resistor, 30K, 5%, 1/4W		RCR07G303JS
R2, 30, 42	Resistor, 3K, 5%, 1/4W		RCR07G302JS
R3-22, 24-29,41,42, R45,46,47,31	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R32	Resistor, 1.5K, 1%		RN60C1501F
R33	Resistor, 1K, Var.	Beckman	89WR1K
R34	Resistor, 1.2M, 1%		RN60C1244F
R35	Resistor, 500K, Var.	Beckman	89WR500K
R36, 38	Resistor, 1K, 1%		RN60C1001F
R37	Resistor, 20K, 1%		RN60C2002F
R44,40,39,48	Resistor, 1K, 5%, 1/4W		RCR07G102JS
C1	Capacitor, 10µf, 16V, EL	Sprague	TE-1155E
C2	Capacitor, .1µf, Disc.	Centralab	UK-16-104
C3,15,12,5,6,7,8,9, C16, 17, 4, 10	Capacitor, .01µf, Disc.	Centralab	UK-16-103
C11	Capacitor, 33µf, 10V, Tant, 20%	Sprague	196D336X9010KA1
C14	Capacitor, .1µf, 5%, Polycarb	Siemens	B32561-0.1/5/250
CR1	Diode Sign.		1N4148
C18	Capacitor, 200pf, Silver Mica		CM04FD201J03
RECEIVER REFERENCE MODULE (A10)			
U4, 9, 16	Dual D-Type Flip Flop		SN74LS74AN
U5, 6	Dual JK-Type Flip-Flop		SN74LS73N
U15,13,2,3	Dual 4 Input NAND		SN74LS00N
U10, 11, 17	BCD Counter		SN74LS161AN
U14	Line Receiver		SN75107AN
U7	Line Driver		SN75452BP
U12, 8	Dual One Shot		SN74LS123N
U1	Hex Inverter		SN74LS04N

REF. DES.	COMPONENT DESCRIPTION	COMPONENT MANUFACTURER	PART NO.
RECEIVER REFERENCE MODULE (A10) (Con't)			
R9, 10	Resistor, 180, 5%, 1/4W		RCR07G181JS
R15, 16, 19, 21	Resistor, 10K, 5%, 1/4W		RCR07G103JS
R11, 12	Resistor, 47, 5%, 1/4W		RCR07G371JS
R14,13,8,6,5,1,18,22, R23, 24	Resistor, 1K, 5%, 1/4W		RCR07G102JS
R17	Resistor, 10, 5%, 1/4W		RCR07G100JS
R7	Resistor, 6.8K, 5%, 1/4W		RCR07G682JS
R20	Resistor, 7.5K, 5%, 1/4W		RCR07G752JS
R2	Resistor, 75, 5%, 1/4W		RCR07G750JS
R3	Resistor, 23.7K, 1%, 1/4W		RN60C2372F
R4	Resistor, 6.81K, 1%, 1/4W		RN60C6811F
C6	Capacitor, 150pf	RMC	CM150PF N150 5%
C5	Capacitor, 75pf	RMC	CG75PF N030 5%
C21	Capacitor, 20pf, Silver Mica	Sprague	CM04ED200J03
C10,7,13,14,17,18,22	Capacitor, .1µf, 20V, Disc.	Centralab	UK-16-104
C2	Capacitor, 3900pf, Silver Mica	Sprague	CM06FD392J03
C3, 4	Capacitor, 47µf, 6V, Tant., 10%	Sprague	150D476X9006B2
C19, 20	Capacitor, 10µf, 16V, EL	Sprague	TE-1155E
C15, 16	Capacitor, 12pf, Silver Mica	Sprague	CM04CD120J03
C11, 12	Capacitor, 1-18pf, Glass	Sprague-Goodman	GGC-18000
Places Marked "C"	Capacitor, .01µf, @ 16V EL	Centralab	UK-16-103
CR1, 2	Diode, SIgn.		1N4148
L4, 5	Coil, 100µh	Lenox Fugle	NR-100/LF-100
L3	Coil, 330µh	Lenox Fugle	NR-330/LF-330
L1, 2	Coil, 49µh, Adj.	Aladdin	B6346
Q1-6	Transistor, NPN		2N3904
TP1-8	Terminals	Cambion	2027-2
R25, 26	Resistor, 2K, 1/4W, 5%		RCR07G202JS
C8	Capacitor, 22pf	RMC	CG22PF NPO
C9	Capacitor, 20pf	RMC	CG20PF N1500